MAXIM

RR-1L

January 1999

Product Reliability Report

This report presents the product reliability data for Maxim's analog products. The data was acquired from extensive reliability stress testing performed in 1997/1998. It is separated into seven fabrication processes: 1) Standard Metal-Gate CMOS (SMG); 2) Medium-Voltage Metal-Gate CMOS (MV1); 3) Medium-Voltage Silicon-Gate CMOS (MV2); 4) 3µm Silicon-Gate CMOS (SG3); 5) 5µm Silicon-Gate CMOS (SG5); 6) 1.2µm Silicon-Gate CMOS (SG1.2); and 7) Bipolar Processes (BIP).

Over 11 million device hours have been accumulated for products stressed at an elevated temperature (135°C) during this period. Data in this report is typical of Maxim production, and demonstrates the consistently high reliability of Maxim products.

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Fabrication Processes

Maxim currently uses the seven fabrication processes described below. Appendix 3 gives other pertinent information and shows cross-sectional views of these processes.

SMG (Standard Metal-Gate CMOS)

SMG is a 6µm, 24V, metal-gate CMOS process. It has conservative design rules, but is appropriate for many SSI and MSI circuit designs. This very popular fabrication process is used to produce many of Maxim's products.

MV1 (Medium-Voltage Metal-Gate CMOS)

MV1 is a 12µm, 44V, metal-gate CMOS process, used exclusively to produce our analog switch product line.

MV2 (Medium-Voltage Silicon-Gate CMOS)

MV2 is a 5µm, 44V, silicon-gate CMOS process, also used in our analog switch production line.

SG3, SG5, and SG1.2 (3µm, 5µm, and 1.2µm Silicon-Gate CMOS)

SG3 is a 3µm, 12V, silicon-gate CMOS process. SG5 is a 5µm, 20V, silicon-gate CMOS process. SG1.2 is a 1.2µm, 6V, silicon-gate CMOS process. SG1.2 has become our present process standard. Further processes are under development at Maxim.

Bipolar (12µm and 18µm)

Bipolar is a 12µm, 24V or 18µm, 44V bipolar process used chiefly for precision references, op amps, and A/D converters.

Reliability Methodology

Maxim's quality approach to reliability testing is conservative. Each of the seven fabrication processes has been qualified using the following industry-standard tests: Life Test, 85/85, Pressure Pot, HAST, High-Temperature Storage Life, and Temperature Cycling **(Table 1)**. Each process has been qualified and proven to produce inherently high-quality products.

Maxim's SMG, MV1, MV2, SG3, SG5, SG1.2, and Bipolar processes clearly meet or exceed the performance and reliability expectations of the semiconductor industry. Results of Maxim's long-term life testing on our various process technologies are summarized in **Table 2**. These processes are qualified for production. Cross-sectional views of these seven processes are shown in **Figures 1-7**.

TABLE 1. MAXIM PROCESS RELIABILITY TESTS

TEST NAME	CONDITIONS	SAMPLING PLAN ACC/SS
Life Test	+135°C, Biased, 1000 hrs.	1/77
85/85	+85°C, 85% R.H., Biased, 1000 hrs.	1/77
HAST	+120°C, 85% R.H., Biased, 100 hrs.	1/77
Pressure Pot	+121°C, 100% R.H., 2 ATM, Unbiased, 168 hrs.	0/77
Temperature Cycling	-65°C to +150°C, Air-to-Air, Unbiased, 1000 cycles	1/77
High-Temp. Storage	+150°C, Unbiased, 1000 hrs.	1/77

TABLE 2. LIFE TEST RESULT OF MAXIM PRODUCTS FOR EACH PROCESS
(+135°C, 1000 Hours, 60% UCL)

PROCESS FAMILY	SAMPLE SIZE	REJECTS	FIT AT 25°C	FIT AT 55°C
SMG	2617	0	0.08	1.37
MV1	539	1	0.85	14.6
MV2	462	1	0.99	17.2
SG3	1741	1	0.26	4.55
SG5	1305	1	0.35	6.07
SG1.2	3118	0	0.06	1.15
BIP	1258	1	0.36	6.29
Totals	**11040**	**5**	**0.13**	**2.23**

Product Reliability Report

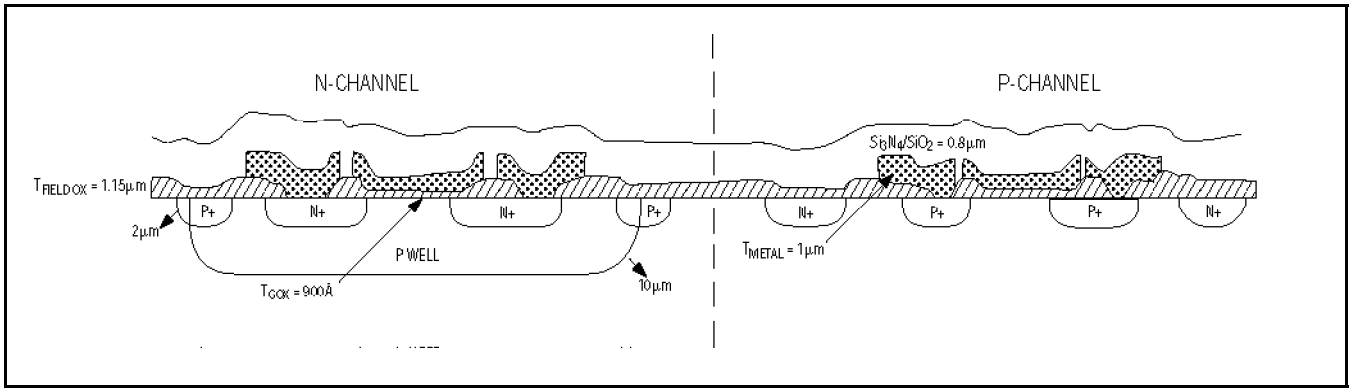

Figure 1. SMG Process

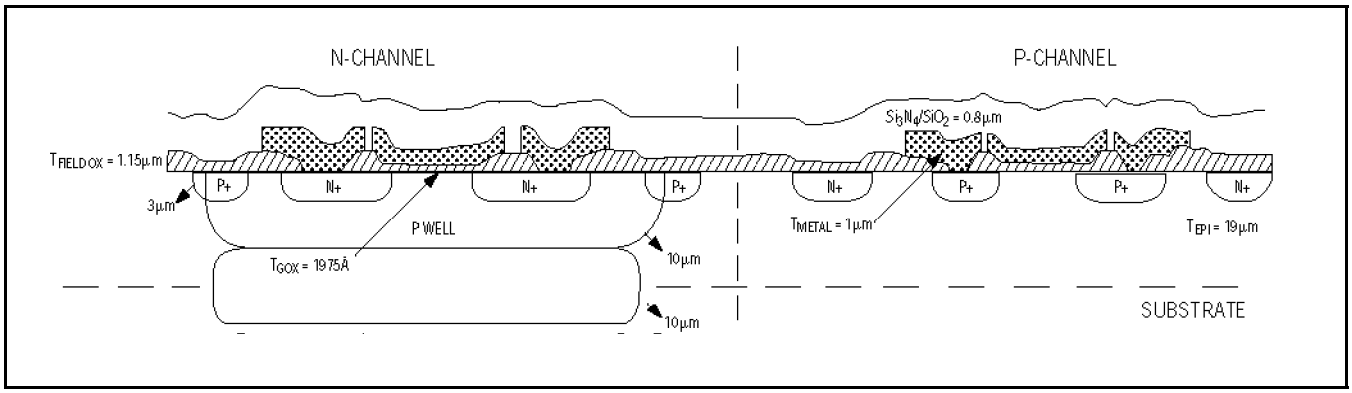

Figure 2. MV1 Process

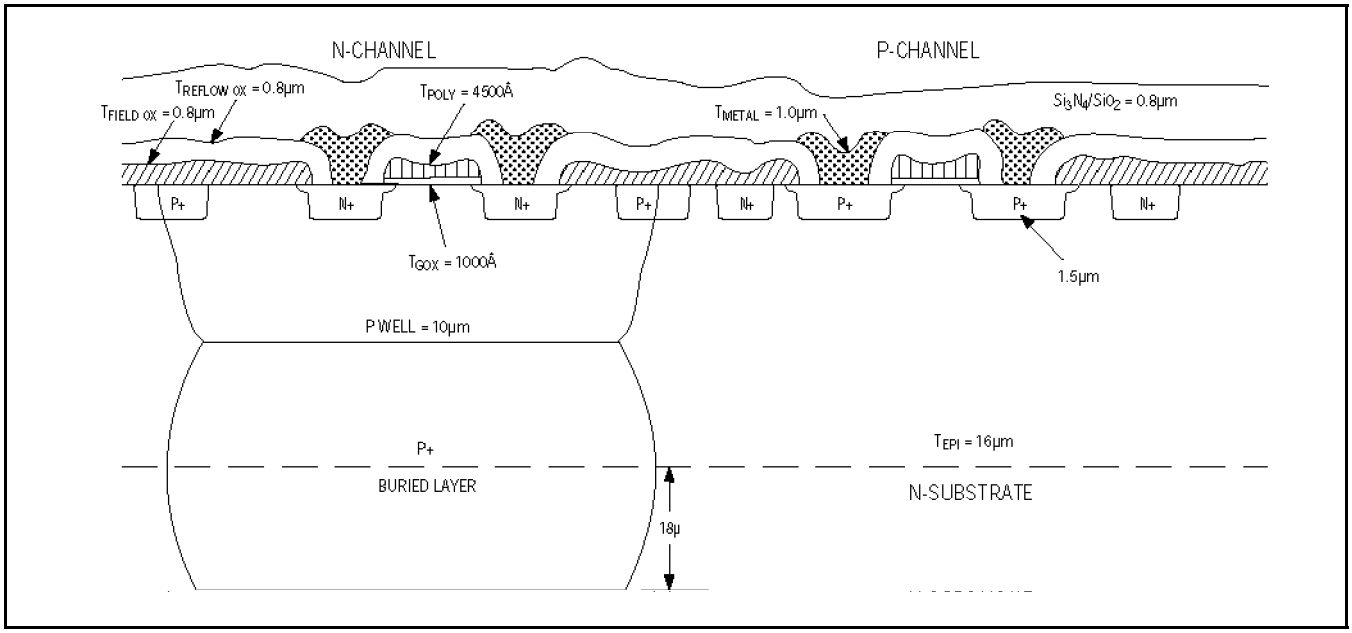

Figure 3. MV2 Process

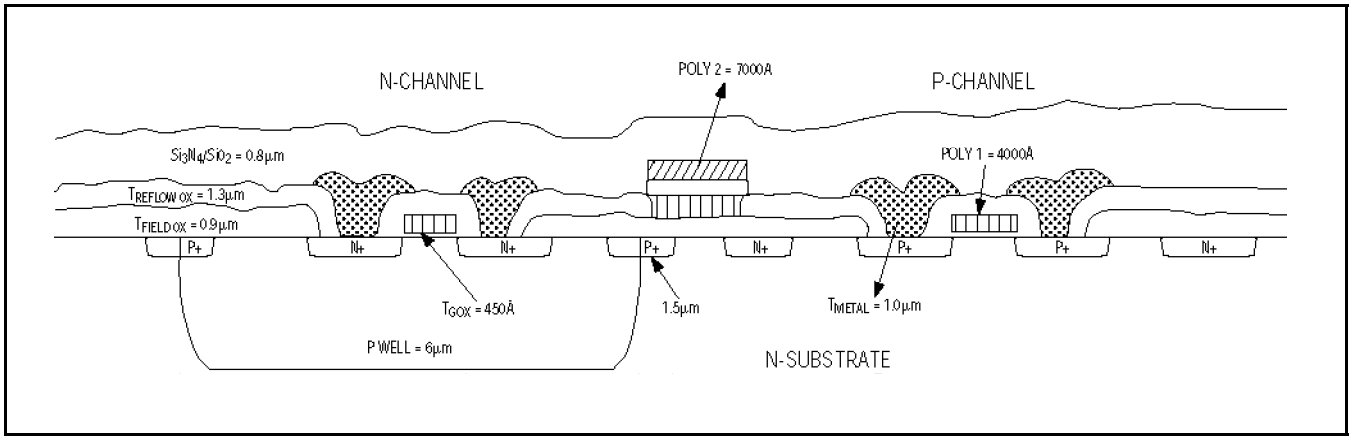

Figure 4. SG3 Process

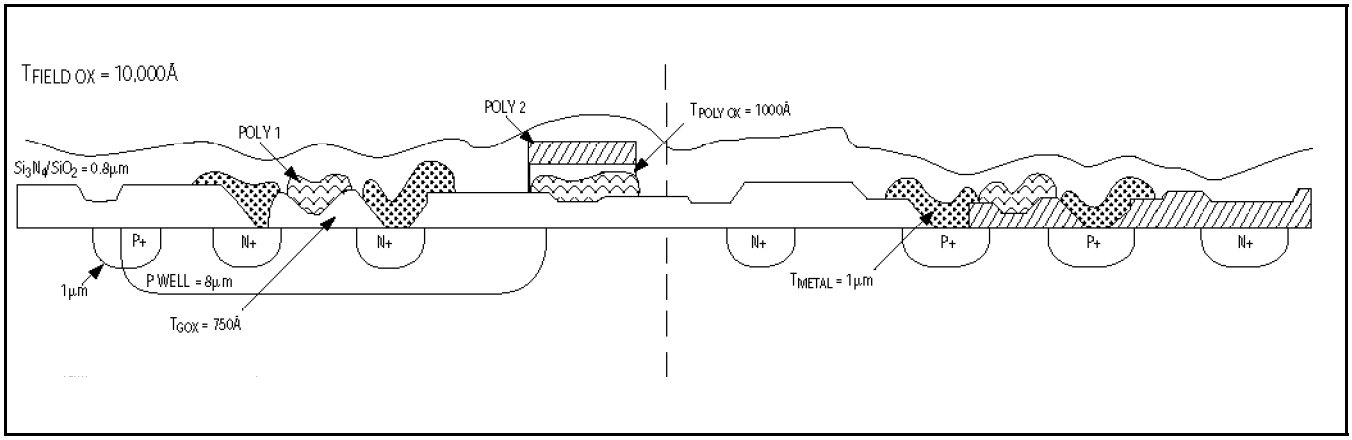

Figure 5. SG5 Process

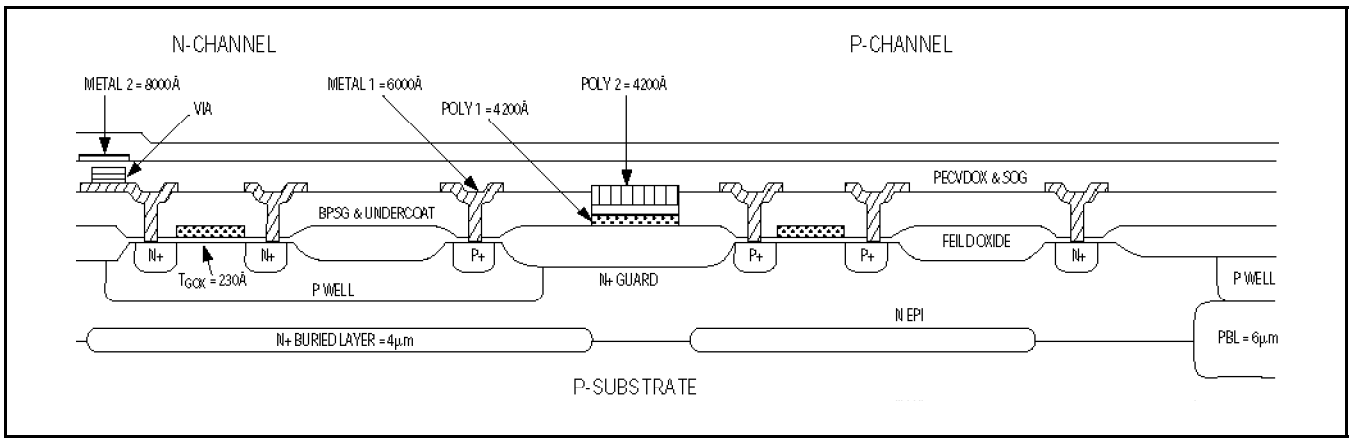

Figure 6. SG1.2 Process

Product Reliability Report

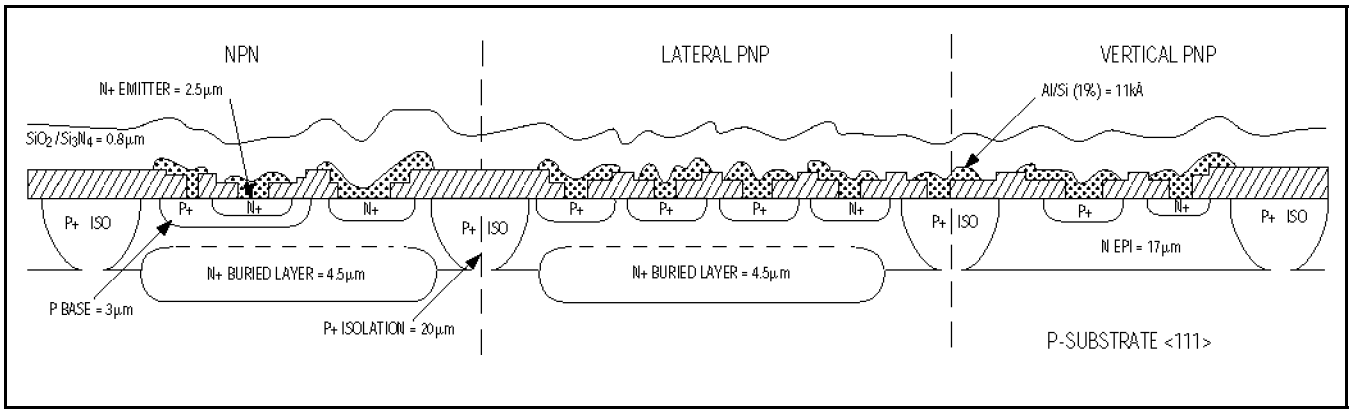

Figure 7. BIP Process

Reliability Program

Reliability Program Steps

Maxim has implemented a series of Quality and Reliability programs aimed at building the highest quality, most reliable analog products in the industry. All products, processes, packages, and manufacturing changes must be subjected to Maxim's reliability testing before release to production manufacturing. Our reliability program includes the following steps:

Step 1: Initial Reliability Qualification Program

Maxim's product reliability test program meets EIA-JEDEC standards and most standard OEM reliability test requirements.

Table 1 summarizes the qualification tests that are part of Maxim's reliability program. Before releasing products, we require that three consecutive manufacturing lots from a new process technology successfully meet the reliability test requirements.

Step 2: Ongoing Reliability Monitor Program

Every week Maxim identifies wafer lots from each process to be the subjects of reliability monitor testing. Each lot is tested to 48 hours of High-Temperature Operating Life (HTOL) at 135°C. Every quarter, one wafer lot per process per fab is subjected to the same long-term reliability tests as defined in Table 1, which include HTOL, 85/85, Pressure Pot, Temperature Cycling, and High Temperature Storage. Test results are fed back to production.

Step 3: In-Depth Failure Analysis and Corrective Action

Our technical failure-analysis staff is capable of analyzing every reliability test failure to the device level. If an alarming reliability failure mechanism or trend is identified, the corrective action is initiated automatically. This proactive response and feedback ensures that discrepancies in any device failure mechanism are corrected before becoming major problems.

Designed-In Reliability

A disciplined design methodology is an essential ingredient of manufacturing a reliable part. No amount of finished-product testing can create reliability in a marginal design. To design in reliability, Maxim began by formulating a set of physical layout rules that yields reliable products, even under worst-case manufacturing tolerances. These rules are rigorously enforced, and every circuit is subjected to computerized Design Rule Checks (DRCs) to ensure compliance.

Special attention is paid to Electrostatic Discharge (ESD) protection. Maxim's goal is to design every pin of every product to withstand ESD voltages in excess of 2000V, through a unique protection structure. In the case of our RS-232 interface circuits, certain devices can even withstand ±15kV ESD on I/O pins, using the Human Body Model; ±8kV ESD using the IEC1000-4-2 Contact Discharge method; or ±15kV ESD using the IEC1000-4-2 Air-Gap Discharge method. Maxim tests each new product design for 50mA latchup protection.

Designs are extensively simulated (using both circuit and logic simulation software) to evaluate performance under worst-case conditions. Finally, every design is checked and rechecked by independent teams before being released to mask making.

Wafer Inspection

All wafers are fabricated using stable, proven processes with extremely tight control. Each wafer must pass numerous in-process checkpoints (such as oxide thickness, alignment, critical dimensions, and defect densities), and must comply with Maxim's demanding electrical and physical specifications.

Finished wafers are inspected optically to detect any physical defects. They are then parametrically tested to ensure full conformity to Maxim's specifications. Our parametric measurement system is designed to make the precision measurements that will ensure reliability and reproducibility in analog circuits.

We believe our quality-control technology is the best in the industry, capable of resolving current levels below 1pA, and of producing less than 1pF capacitance. Maxim's proprietary software allows automatic measurement of subthreshold characteristics, fast surface-state density, noise, and other parameters crucial to predicting long-term stability and reliability. Every Maxim wafer is subject to this rigorous screening at no premium to our customers.

Reliability Data

Failure-Rate History

Figure 8 illustrates Maxim's Failures-in-Time (FIT) rate performance based on the Life Test Data summary in **Table 3**. It also highlights the progressive improvements made in reliability, a trend that we expect to continue, due to our continuous-improvement methodology.

Infant Mortality Evaluation

Maxim evaluates each process and product family's Infant Mortality rate immediately after achieving qualified status. Through Infant Mortality analysis,

TABLE 3. RELIABILITY DATA SUMMARY BY PRODUCT LINE

PRODUCT LINE	LOTS TESTED	FAILURES	TOTAL UNITS TESTED	FITS AT 25°C 60% UCL	FITS AT 25°C 90% UCL
Converters (A/D, D/A)	18	2	1408	1.17	1.99
Linear (i.e., Op Amp)	141	25	11,157	1.27	1.54
Total	**159**	**27**	**12,565**	**1.22**	**1.46**

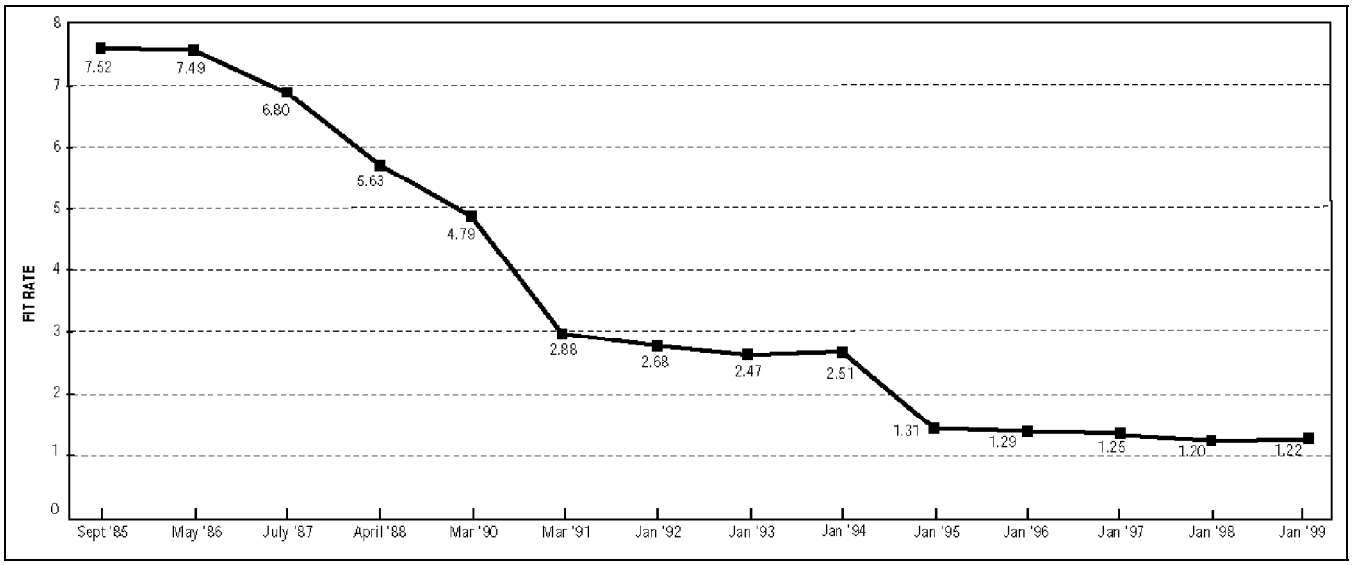

Figure 8. Maxim FIT Rates Over Time

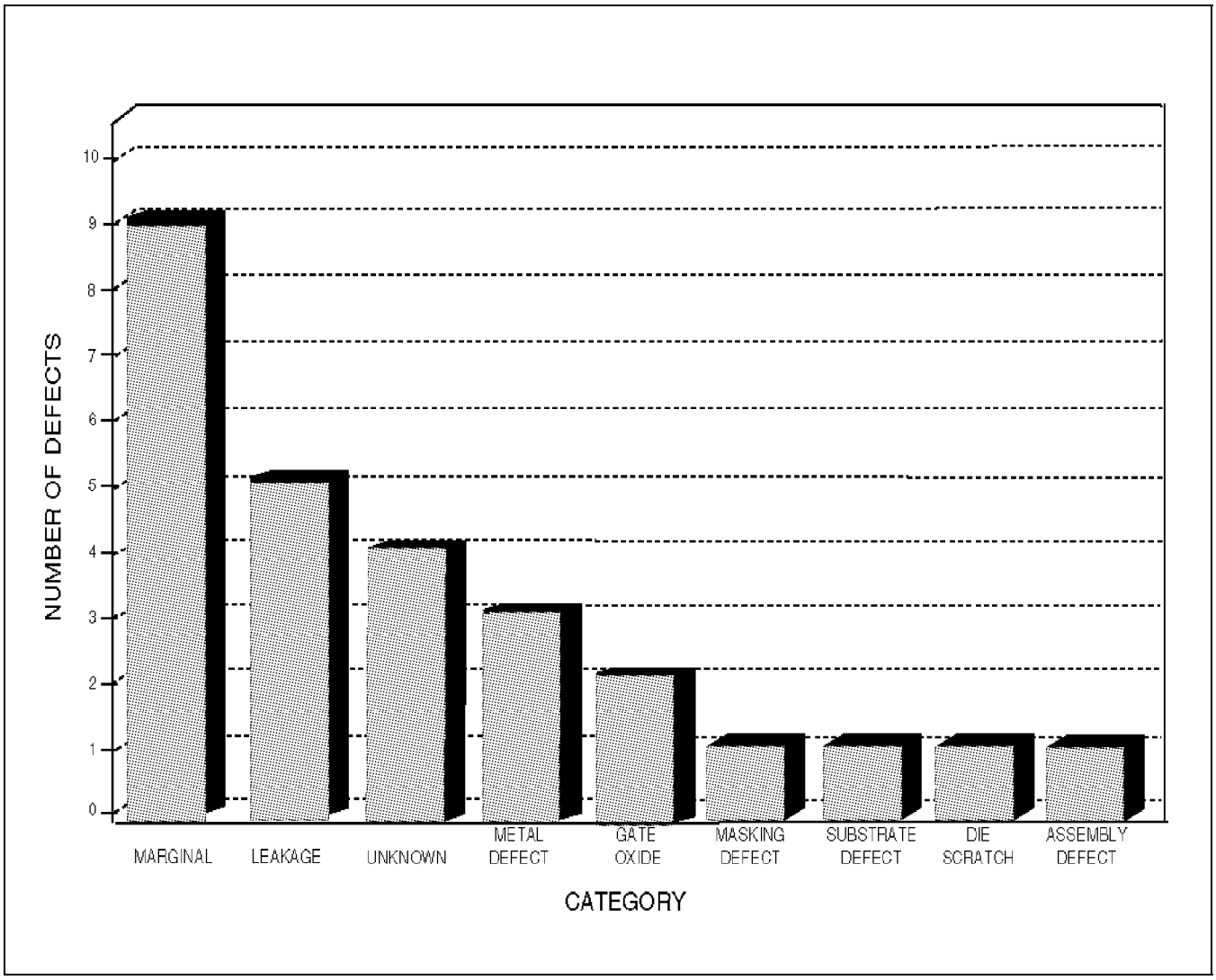

Figure 9. Infant Mortality Pareto Chart

TABLE 4. INFANT MORTALITY EVALUATION RESULTS (BI Temperature = 135°C)

PRODUCT	LOT	SS	FAILURES	PPM	ANALYSIS
		SMG Process			
MAX232CPE	NHUBBZ133E	1000	0	0	
MAX232CPE	NHUBBZ137C	500	0	0	
MAX232CPE	NHUBBZ151A	500	0	0	
MAX232CPE	NHUBAZ152	500	0	0	
MAX232CPE	NHUBBZ038D	1095	0	0	
MAX202CPE	NHUADZ133F	500	0	0	
MAX208CNG	NYCAGO133E	500	0	0	
MAX208CNG	NYCAGO138C	500	0	0	
MAX208CNG	NYCAGZ176E	500	0	0	
MAX241CWI	NKDADO468F	600	0	0	
Subtotals		**6195**	**0**	**0**	
MAX232ECPE	NDOACB061C	1000	0	0	
MAX232ECPE	NDOACN101D	500	0	0	
MAX241ECWI	NKUCFO618Q	500	0	0	
MAX241ECWI	NKUCEO639Q	500	0	0	
Subtotals		**2500**	**0**	**0**	
MAX202EEPE	NDOBCB050G	1000	0	0	
MAX202ECPE	NDOBCN119A	1000	0	0	
MAX202EEPE	NDOBCZ135	1000	0	0	
MAX202ECPE	NDOBCN160C	1000	0	0	
Subtotals		**4000**	**0**	**0**	
MAX1232CPA	NPPADZ124C	1000	0	0	
Subtotals		**1000**	**0**	**0**	
MAX691CPE	NPYADA338C	1000	0	0	
MAX691EPE	NPYADA362C	1000	0	0	
MAX691CPE	NPYADA414C	1000	0	0	
MAX691CPE	NPYADA460C	500	0	0	
MAX691CPE	NPYADA464B	500	0	0	
MAX694CPA	NPYCDB286B	1000	0	0	
MAX694CPA	NPYCDB304H	1000	0	0	
MAX695EPE	NPYCDB236E	1000	0	0	
Subtotals		**7000**	**0**	**0**	
MAX622CSA	NPQABO032A	500	0	0	
Subtotals		**500**	**0**	**0**	
MAX850ESA	XCOAFS273A	1000	0	0	
MAX850ESA	XCOAFB332A	999	0	0	
MAX850ESA	XCOAFB390A	992	0	0	
MAX850CSA	XCOAFA406A	450	0	0	
MAX850ESA	XCOAFA591A	1000	0	0	
Subtotals		**4441**	**0**	**0**	
MAX1406CPE	XC4ABZ009C	500	0	0	
MAX3185CWP	XPEACZ057C	500	0	0	
ICL7665ACPA	NYUADO020E	500	0	0	
Subtotals		**1500**	**0**	**0**	
		MV1 Process			
DG211CJ	XRCACB228B	1000	1	1000	ID_{ON} leakage
DG211CJ	XRCACB234B	1000	0	0	
DG211CJ	XRCACB284D	1000	0	0	
DG211CJ	XRCACN305B	1000	1	1000	I_{DS} leakage
Subtotals		**4000**	**2**	**500**	
		MV2 Process			
DG411DJ	XRLADS087A	951	0	0	
DG411DJ	XRLADB102B	1000	0	0	
DG412DJ	XRLBDB116A	1000	0	0	
DG412DJ	XRLBDB119L	1000	0	0	
DG413DJ	XRLCDB126J	1000	0	0	
DG412DJ	XRLBDA160A	500	0	0	
Subtotals		**5451**	**0**	**0**	
		SG3 Process			
MAX297EPA	NGKECB038C	1275	0	0	
MAX293CPA	XGKBJA115B	1200	0	0	
Subtotals		**2475**	**0**	**0**	
MAX3232CPE	NDMCBZ083Q	600	0	0	
MAX3223CPP	NDMBCZ116	500	0	0	
MAX3243CAI	NDLBFZ297	1000	0	0	
Subtotals		**2100**	**0**	**0**	
MAX485CPA	NKNAEB139D	1000	1	1000	Die scratch
MAX483CPA	NKNCFB148A	1000	0	0	
MAX485CPA	NKNAEN197C	1000	0	0	
Subtotals		**3000**	**1**	**333**	
MAX483ECPA	XIKCBB042G	997	0	0	
MAX491ECPD	XIKEBZ136C	500	0	0	
Subtotals		**1497**	**0**	**0**	

TABLE 4. INFANT MORTALITY EVALUATION RESULTS (BI Temperature = 135°C) *(continued)*

PRODUCT	LOT	SS	FAILURES	PPM	ANALYSIS
MAX640CPA	NSUBDB039A	500	0	0	
MAX660CPA	NYIAEO143A	500	0	0	
MAX660CPA	NYIAEC162A	1000	0	0	
MAX705EPA	NTOAEZ145A	985	0	0	
MAX706EPA	NTOBFB291B	1000	0	0	
MAX691ACPE	NTYBLB089E	1489	0	0	
MAX708EPA	NTODFA320D	1000	0	0	
MAX709TCPA	NRHCBO169Q	500	0	0	
MAX709LCPA	NRHABO261M	500	0	0	
MAX709LCPA	NRHABO264L	500	0	0	
MAX712EPE	NAABED030B	993	0	0	
Subtotals		**8967**	**0**	**0**	
MAX782CBX	XTNAFG770A	495	0	0	
MAX785CAI	XCFAHZ300D	500	0	0	
MAX797CSE	XCUBDB669A	996	0	0	
MAX797CSE	XCUBDA772A	1000	1	1000	MARGINAL V_{REF}
MAX8213ACSE	NAGAGB053A	1000	0	0	
MAX860CPA	NDKADZ158F	500	0	0	
Subtotals		**4491**	**1**	**222**	
SG5 Process					
MAX191BCNG	XZRBQA166A	2171	0	0	
MAX232ACPE	XETAHN121C	1000	0	0	
MAX232ACPE	XETAHN191C	1000	0	0	
MAX232ACPE	XETAHA803A	1000	0	0	
MAX232ACPE	XETAHN885A	1000	0	0	
MAX232ACPE	XETAHN999D	1000	0	0	
MAX232AEPE	NETAIZ001B	1000	0	0	
MAX232ACPE	NETAHN319A	500	0	0	
MAX232ACPE	NETAIQ002Q	1000	0	0	
MAX232ACPE	XETAHN278A	500	0	0	
MAX391CPE	XDJACZ001D	1000	0	0	
MAX395CNG	XKDABZ108A	500	0	0	
Subtotals		**11,671**	**0**	**0**	
MAX543BEPA	XLUABA078D	500	1	2000	SUBSTRATE DEFECT
MAX543ACPA	XLVABA082A	1000	1	1000	GATE OXIDE DEFECT
MAX543ACPA	NLVACZ001A	1000	0	0	
MAX734CPA	NSDAEZ003B	1000	0	0	
MX7523KN	XXKDJA057E	1000	1	1000	GATE OXIDE DEFECT
MX7523JN	XXKDJA058B	2000	0	0	
MX7534KN	XDWADA025A	540	0	0	
MX7545JN	XXLABZ056Q	600	0	0	
MX7543KN	NXLDCZ001A	1641	0	0	
Subtotals		**9281**	**3**	**323**	
SG1.2 Process					
MAX549ACPA	NMVBCA007Q	2000	0	0	
MAX619CPA	USEAGB007A	500	0	0	
MAX619CPA	JSEAMQ001A	1000	0	0	
MAX619CPA	JSEAHX002A	1000	0	0	
MAX619CPA	JSEAHB003A	500	0	0	
MAX619CPA	JSEAHA079A	600	0	0	
MAX619CPA	JSEAMA182C	1000	0	0	
MAX619EPA	JSEAMA250A	500	0	0	
MAX6160ESA	NE2ECX002G	2000	0	0	
MAX811LCPA	BGTADS003A	528	0	0	
MAX818LCPA	BJSCCC013E	965	0	0	
MAX849ESE	NIPCGB014K	500	0	0	
MAX849ESE	NIPCEB012A	1000	0	0	
MAX887HESA	IHJCHA017A	1000	0	0	
MAX887HESA	NHJCGA021D	1000	0	0	
MAX887HESA	NHJCGA022A	500	0	0	
MAX890LESA	NLCBFQ002A	500	0	0	
MAX890LESA	NLCBHB025F	998	1	1002	1-LEAKAGE, CAUSE UNKNOWN
MAX890LESA	IX3BAV029A	500	0	0	
MAX890LESA	NLCBHA033A	1000	0	0	
MAX1603EAI	NLFADO001I	745	0	0	
MAX7219ENG	NDRAES001Q	1199	1	834	1-UNKNOWN
MAX1617MEE	NXSAHA037B	5029	2	398	2-UNKNOWN
MAX1617MEE	NXSAHS038A	4880	6	1230	3-MARGINAL 1-LEAKAGE 1-MASKING 1-ASSEMBLY
MAX1617MEE	NXSAHR040A	4848	6	1238	3-MARGINAL 3-METAL DEFECT
MAX1617MEE	NXSAHS042F	4004	3	749	1-MARGINAL 2-LEAKAGE
Subtotals		**38,296**	**19**	**496**	

TABLE 4. INFANT MORTALITY EVALUATION RESULTS (BI Temperature = 135°C) *(continued)*

PRODUCT	LOT	SS	FAILURES	PPM	ANALYSIS
BIP Process					
MAX400CPA	GFGAEA003G	994	0	0	
MAX400CPA	GFGAEO006A	500	0	0	
MAX472CPA	GBXBDO042C	1000	0	0	
MAX492EPA	HCMADZ001B	567	1	1763	V_{OS}
MX581KH	GHPAMB007N	1000	0	0	
MAX779LCPA	HSSCJX001B	950	0	0	
MAX873BCPA	GHRAGQ001F	850	0	0	
MAX872EPA	MHQAFB047D	1000	0	0	
MAX872CPA	GHQAGO005A	500	0	0	
MAX872CPA	GHQAGB019C	500	0	0	
MAX873BCPA	GHRAGA004C	1000	0	0	
MAX874EPA	GHQBGB016J	801	0	0	
Subtotals		**9662**	**1**	**103**	
MAX724CCK	MXGAIB020A	1000	0	0	
MAX724CCK	MXGAIB026C	1000	0	0	
MAX724CCK	GXGAJX005A	938	0	0	
MAX727CCK	GAHBIB013D	1000	0	0	
Subtotals		**3938**	**0**	**0**	
MAX913CPA	HWNADB007A	1000	0	0	
MAX913CPA	HWNADB009E	1000	0	0	
MAX913EPA	HWNADB026E	1000	0	0	
MAX913CPA	HWNADC029B	500	0	0	
MXL1001CN8	GFGAEZ005A	1500	0	0	
Subtotals		**5000**	**0**	**0**	
Combined Totals		**136,965**	**27**	**197**	

we can identify the common defects for each process or product family. For an illustration of Maxim's low Infant Mortality rate, refer to **Table 4**. **Figure 9** is an Infant Mortality pareto chart showing each category of failures; categories are prioritized based on relative frequency.

Merits of Burn-In

Maxim's early conservative approach included burn-in as a standard stage of our production flow. Burn-in ensured that our customers were receiving a quality product. Now, with the addition of our own sophisticated fabrication facilities, we have improved the innate product quality to the point where burn-in adds little reliability value.

Each time a new fabrication process is introduced at Maxim, an Infant Mortality (burn-in) evaluation is initiated with the process qualification. Through this Infant Mortality evaluation, we can identify fabrication process defects at an early stage of production. Using the data in Table 4 (Infant Mortality Evaluation Results) and Figure 9 (Infant Mortality Pareto Chart), we can determine which category should next be improved. The data shown demonstrates the positive direction of Maxim's quality standards. It illustrates our continued dedication to providing the lowest overall-cost solution to our customers through superior quality products.

The data of Table 2 summarizes the reliability effects of production burn-in. Essentially, only five units out of 11,040 were found to be outside their specifications after 1000 hours of operation at 135°C. This is equal to a FIT rate of 0.13 at 25°C.

In comparison, the Infant Mortality rate is equal to 27 units out of 136,965 after 12 hours at 135°C, which has an equivalent FIT rate of approximately 0.84. In practical terms, 0.0197% of the total population would be found as defective through the first six years of operation (below 0.0033%/year), with an additional 0.009%/year failing over the remaining life of the product.

Life Test at 135°C

Life Test is performed using biased conditions that simulate a real-world application. This test estimates the product's field performance. It establishes the constant failure-rate level and identifies any early wearout mechanisms. The tested product is kept in a controlled, elevated-temperature environment, typically at 135°C. This test can detect design, manufacturing, silicon, contamination, metal integrity, and assembly-related defects.

Test Used:	High-Temperature Life and Dynamic Life Test (DLT)
Test Conditions:	135°C, 1000 hrs., inputs fed by clock drivers at 50% duty cycle, or static
Failure Criteria:	Must meet data sheet specifications
Results:	See Tables 5–11

Humidity Tests

The most popular integrated circuit (IC) packaging material is plastic. Plastic packages are not hermetic, therefore moisture and other contaminants can enter the package. Humidity testing measures the contaminants present and the product's resistance to ambient conditions. Contaminants can be introduced during both wafer fabrication and assembly, and they can negatively affect product performance. Pressure Pot, 85/85, and HAST tests are used for this evaluation.

85/85 Test

Maxim tests plastic-encapsulated products with an 85/85 test to determine the moisture resistance of our products under bias conditions. This test can detect the failure mechanisms found in Life Test. In addition, it can detect electrolytic and chemical corrosion.

Test Used:	85/85
Test Conditions:	85°C, 85% Relative Humidity (RH), biased,1000 hrs.
Failure Criteria:	Must meet data sheet specifications
Results:	See Table 12

Pressure Pot Test

This test simulates a product's exposure to atmospheric humidity, which can be present during both wafer fabrication and assembly. Although an IC is covered with a nearly hermetic passivation layer (upper-surface coat), the bond pads must be exposed during bonding.

Test Used:	Pressure Pot
Test Conditions:	121°C, 100% RH, no bias, 168 hrs.
Failure Criteria:	Must meet data sheet specifications
Results:	See Table 13

HAST Test

Highly Accelerated Steam and Temperature (HAST) testing often replaces 85/85 testing. It serves the same basic function as 85/85, but permits the evaluation to be completed in 10% of the time, making HAST tests useful for immediate feedback and corrective action.

Test Used:	HAST
Test Conditions:	120°C, 85% RH, biased,100 hrs.
Failure Criteria:	Must meet data sheet specifications
Results:	See Table 14

Temperature Cycling Test

This test measures a component's response to temperature changes and its construction quality. The test cycles parts through a predetermined temperature range (usually -65°C to +150°C). Both fabrication and assembly problems can be discovered using Temperature Cycling, but the test typically identifies assembly quality.

Test Used:	Temperature Cycling
Test Conditions:	-65°C to +150°C, 1000 cycles
Failure Criteria:	Must meet data sheet specifications
Results:	See Table 15

High-Temperature Storage Life Test

This test evaluates product performance after being stored for a set duration (1000 hours) at a high temperature (150°C). It is only useful for failure mechanisms accelerated by heat.

Test Used:	High-Temperature Storage Life
Test Conditions:	150°C, 1000 hrs. unbiased
Failure Criteria:	Must meet data sheet specifications
Results:	See Table 16

Hybrid Products Reliability Data

Maxim's hybrid product reliability data is presented in **Tables 17 and 18**. Table 17 is the Life Test data for hybrid products tested. Table 18 is the Temperature Cycling test data for hybrid products.

Process Variability Control

Reliability testing offers little value if the manufacturing process varies widely. A standard assumption, which is often false, is that test samples pulled from production are representative of the total population. Sample variability can be lessened by increasing the number of samples studied. However, unless a process is kept "in control," major variations can invalidate reliability test results, leading to incorrect conclusions and diminishing the integrity of failure rate estimates. Uncontrolled processes also make it difficult to prove failure rates of less than 10 FIT.

Maxim monitors the stability of critical process parameters through the use of computerized Statistical Process Control (SPC). Over 125 charts are monitored in-line during wafer production. Additionally, over 100 process parameters are monitored at Wafer Acceptance. Maxim has a target Capability Coefficient (Cpk) goal of 1.3, which is nearly 32 ppm. In addition to SPC, Maxim uses Design of Experiments (DOE) to improve process capability, optimize process targeting, and increase robustness.

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Reliability Test Results

Tables 5–18 list the results of reliability tests Maxim has performed for various packages.

TABLE 5. LIFE TEST RESULTS AT 135°C/1000 HRS. FOR THE METAL-GATE CMOS PROCESS (SMG)

DEVICE TYPE	DATE CODE	PKG.	SAMPLE SIZE	FAILURES (HRS)		
				192	500	1000
MAX8211	9650	8 SO	77	0	0	0
MAX232	9701	16 PDIP	77	0	0	0
MAX853	9703	8 SO	100	0	0	0
MAX8211	9712	8 SO	77	0	0	0
MAX207	9718	24 CERDIP	77	0	0	0
MAX213	9720	28 WSO	80	0	0	0
MAX241	9721	28 WSO	80	0	0	0
MAX690	9722	8 PDIP	76	0	0	0
MAX690	9723	8 PDIP	77	0	0	0
MAX232	9724	16 PDIP	77	0	0	0
MAX8211	9724	8 SO	76	0	0	0
MAX241	9730	28 WSO	80	0	0	0
MAX232	9730	16 PDIP	80	0	0	0
MAX208	9734	24 PDIP	80	0	0	0
MAX622	9734	8 SO	80	0	0	0
MAX622	9735	8 SO	80	0	0	0
MAX8211	9735	8 SO	80	0	0	0
MAX8211	9735	8 SO	75	0	0	0
MAX208	9736	24 PDIP	80	0	0	0
MAX850	9737	8 SO	80	0	0	0
MAX232	9739	16 PDIP	77	0	0	0
MAX232	9739	16 CERDIP	45	0	0	0
ICM7217	9742	28 CERDIP	42	0	0	0
MAX213E	9744	28 WSO	80	0	0	0
MAX202E	9744	16 WSO	79	0	0	0
ICL7665	9745	8 PDIP	80	0	0	0
MAX232	9746	16 WSO	80	0	0	0
MAX232	9748	16 WSO	80	0	0	0
MAX8211	9749	8 SO	77	0	0	0
MAX843	9806	8 SO	80	0	0	0
MAX232	9813	16 PDIP	77	0	0	0
MAX8211	9815	8 SO	77	0	0	0
MAX850	9827	8 SO	77	0	0	0
MAX8211	9841	8 SO	77	0	0	0
Totals			**2617**	**0**	**0**	**0**

TABLE 6. LIFE TEST RESULTS AT 135°C/1000 HRS FOR THE MEDIUM-VOLTAGE METAL-GATE CMOS PROCESS (MV1)

DEVICE TYPE	DATE CODE	PKG.	SAMPLE SIZE	FAILURES (HRS)			NOTES
				192	500	1000	
DG381	9651	14 PDIP	77	0	0	0	
DG211	9715	16 PDIP	77	0	0	1	Parametric failure
DG381	9722	14 PDIP	77	0	0	0	
DG381	9738	14 PDIP	77	0	0	0	
DG381	9803	14 PDIP	77	0	0	0	
DG211	9826	16 PDIP	77	0	0	0	
DG201	9839	16 PDIP	77	0	0	0	
Totals			**539**	**0**	**0**	**1**	

TABLE 7. LIFE TEST RESULTS AT 135°C/1000 HRS. FOR THE MEDIUM-VOLTAGE SILICON-GATE CMOS PROCESS (MV2)

DEVICE TYPE	DATE CODE	PKG.	SAMPLE SIZE	FAILURES (HRS)			NOTES
				192	500	1000	
DG442	9702	16 PDIP	77	0	0	0	
DG445	9715	16 PDIP	77	0	0	0	
DG445	9722	16 PDIP	77	0	0	0	
DG445	9730	16 PDIP	77	0	0	1	Substrate defect
DG411	9751	16 PDIP	77	0	0	0	
DG411	9820	16 PDIP	77	0	0	0	
Totals			**462**	**0**	**0**	**1**	

TABLE 8. LIFE TEST RESULTS AT 135°C/1000 HRS. FOR THE 3µm SILICON-GATE CMOS PROCESS (SG3)

DEVICE TYPE	DATE CODE	PKG.	SAMPLE SIZE	FAILURE (HRS)			NOTES
				192	500	1000	
MAX706	9651	8 PDIP	77	0	0	0	
MAX4544	9703	8 PDIP	70	0	0	0	
MAX3222	9708	18 PDIP	80	0	0	0	
MAX706	9711	8 PDIP	77	0	0	0	
MAX3232	9724	16 PDIP	80	0	0	0	
MAX706	9724	8 PDIP	77	0	0	0	
MAX660	9734	8 PDIP	80	0	0	0	
MAX1672	9735	16 QSOP	47	0	0	0	
MAX547	9736	44 PLCC	80	0	0	0	
MAX706	9736	8 PDIP	77	0	0	0	
MAX547	9737	44 PLCC	40	0	0	0	
MAX547	9739	44 PLCC	45	0	0	0	
MAX547	9742	44 PLCC	45	0	0	0	
MAX491E	9747	14 PDIP	80	0	1	0	Unknown
MAX708	9751	8 PDIP	77	0	0	0	
MAX797	9807	16 SO	77	0	0	0	
MAX485	9810	8 SO	45	0	0	0	
MAX707	9813	8 PDIP	77	0	0	0	
MAX807	9824	16 PDIP	77	0	0	0	
MAX734	9824	8 PDIP	80	0	0	0	
MAX705	9826	8 PDIP	77	0	0	0	
MAX691A	9836	16 SO	45	0	0	0	
MAX3081	9836	8 PDIP	77	0	0	0	
MAX705	9839	8 PDIP	77	0	0	0	
MAX708	9841	µMAX	77	0	0	0	
Totals			**1741**	**0**	**1**	**0**	

TABLE 9. LIFE TEST RESULTS AT 135°C/1000 HRS. FOR THE 5µm SILICON-GATE CMOS PROCESS (SG5)

DEVICE TYPE	DATE CODE	PKG.	SAMPLE SIZE	FAILURE (HRS)			NOTES
				192	500	1000	
MAX232A	9702	16 PDIP	77	0	0	0	
MAX232A	9716	16 PDIP	77	0	0	0	
MX7533	9726	16 CERDIP	77	0	0	0	
MAX232A	9727	16 PDIP	77	0	0	0	
MX7533	9733	16 CERDIP	45	0	0	0	
MX574	9734	28 CERDIP	45	0	0	0	
MAX734	9734	8 PDIP	80	0	0	1	Unknown
MX574	9735	28 CERDIP	45	0	0	0	
MX7545	9736	20 PDIP	80	0	0	0	
MX7545	9738	20 PDIP	80	0	0	0	
MAX232A	9738	16 PDIP	77	0	0	0	
MAX232A	9752	16 PDIP	77	0	0	0	
MAX232A	9814	16 PDIP	77	0	0	0	
MAX232A	9823	16 PDIP	77	0	0	0	
MAX528	9826	20 PDIP	80	0	0	0	
MX7543	9829	16 PDIP	77	0	0	0	
MAX232A	9838	16 PDIP	80	0	0	0	
MAX232A	9840	16 PDIP	77	0	0	0	
Totals			**1305**	**0**	**0**	**1**	

TABLE 10. LIFE TEST RESULTS AT 135°C/1000 HRS. FOR THE BIPOLAR PROCESS (BIPOLAR)

DEVICE TYPE	DATE CODE	PKG.	SAMPLE SIZE	FAILURE (HRS)			NOTES
				192	500	1000	
REF01	9651	8 PDIP	77	0	0	1	Parametric failure
MAX913	9702	8 PDIP	80	0	0	0	
MAX779	9706	8 PDIP	80	0	0	0	
MAX472	9711	8 PDIP	80	0	0	0	
REF01	9714	8 PDIP	77	0	0	0	
MAX472	9714	8 PDIP	77	0	0	0	
MAX4112	9715	8 SO	80	0	0	0	
MAX472	9716	8 PDIP	80	0	0	0	
MAX4112	9716	8 SO	79	0	0	0	
MXL1001	9720	8 PDIP	80	0	0	0	
MX536	9720	TO100	80	0	0	0	
REF01	9721	8 PDIP	77	0	0	0	
ICL8069	9724	TO52	80	0	0	0	
REF01	9731	8 PDIP	77	0	0	0	
REF02	9821	8 PDIP	77	0	0	0	
REF02	9835	8 PDIP	77	0	0	0	
Totals			**1258**	**0**	**0**	**1**	

TABLE 11. LIFE TEST RESULTS AT 135°C/1000 HRS. FOR THE 1.2µm SILICON-GATE CMOS PROCESS (SG1.2)

DEVICE TYPE	DATE CODE	PKG.	SAMPLE SIZE	FAILURES (HRS)		
				192	500	1000
MAX619	9701	8 PDIP	80	0	0	0
MAX7219	9703	24 PDIP	80	0	0	0
MAX619	9706	8 PDIP	80	0	0	0
MAX7219	9706	24 PDIP	80	0	0	0
MAX619	9707	8 PDIP	80	0	0	0
MAX7219	9708	24 PDIP	80	0	0	0
MAX1603	9717	28 SSOP	60	0	0	0
MAX1630	9717	28 SSOP	80	0	0	0
MAX544	9719	8 PDIP	77	0	0	0
MAX8863	9725	8 PDIP	80	0	0	0
MAX1603	9727	28 SSOP	80	0	0	0
MAX1617	9736	16 QSOP	300	0	0	0
MAX811	9737	8 PDIP	77	0	0	0
MAX1617	9742	16 QSOP	300	0	0	0
MAX1617	9743	16 QSOP	300	0	0	0
MAX1617	9744	16 QSOP	300	0	0	0
MAX849	9745	16 SO	80	0	0	0
MAX619	9801	8 PDIP	80	0	0	0
MAX890	9811	8 SO	80	0	0	0
MAX887	9813	8 SO	77	0	0	0
MAX6160	9815	8 SO	80	0	0	0
MAX1617	9819	16 QSOP	175	0	0	0
MAX1617	9819	16 QSOP	175	0	0	0
MAX1664	9821	20 TSSOP	40	0	0	0
MAX869	8922	16 QSOP	80	0	0	0
MAX1664	9824	20 TSSOP	40	0	0	0
MAX887	9827	8 SO	77	0	0	0
Totals			**3118**	**0**	**0**	**0**

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TABLE 12. 85°C/85% R.H./BIASED, 1000 HRS. (ALL PLASTIC PACKAGES)

DEVICE TYPE	DATE CODE	PKG.	SAMPLE SIZE	FAILURES (HRS)		
				168	500	1000
MAX8211	9650	8 SO	75	0	0	0
REF01	9651	8 PDIP	76	0	0	0
MAX706	9651	8 PDIP	77	0	0	0
DG442	9702	16 PDIP	45	0	0	0
MAX779	9706	8 PDIP	45	0	0	0
MAX619	9706	8 PDIP	45	0	0	0
MAX619	9707	8 PDIP	45	0	0	0
MAX706	9711	8 PDIP	76	0	0	0
MAX8211	9712	8 SO	77	0	0	0
REF01	9714	8 PDIP	77	0	0	0
REF01	9721	8 PDIP	77	0	0	0
DG445	9722	16 PDIP	76	0	0	0
MAX8211	9724	8 SO	76	0	0	0
MAX706	9724	8 PDIP	77	0	0	0
MAX8863	9725	8 PDIP	45	0	0	0
REF01	9731	8 PDIP	45	0	0	0
MAX8211	9735	8 SO	45	0	0	0
MAX706	9736	8 PDIP	45	0	0	0
MAX798	9737	16 SO	77	0	0	0
MAX811	9737	8 PDIP	77	0	0	0
MAX547	9749	44 PLCC	25	0	0	0
MAX708	9751	8 PDIP	45	0	0	0
MAX890	9811	8 SO	45	0	0	0
MAX707	9813	8 PDIP	45	0	0	0
MAX8211	9815	8 SO	45	0	0	0
REF02	9821	8 PDIP	77	0	0	0
MAX734	9824	8 PDIP	77	0	0	0
MAX705	9826	8 PDIP	77	0	0	0
MAX887	9827	8 SO	77	0	0	0
MAX850	9827	8 SO	77	0	0	0
REF02	9835	8 PDIP	45	0	0	0
MAX705	9839	8 PDIP	45	0	0	0
MAX8211	9841	8 SO	45	0	0	0
Totals			**2003**	**0**	**0**	**0**

TABLE 13. PRESSURE POT TEST AT 121°C/100% R.H./ 15 PSIG/168 HRS. (ALL PLASTIC PACKAGES)

DEVICE TYPE	DATE CODE	PKG.	SAMPLE SIZE	FAILURES
MAX8863	9647	5 SOT23	77	0
MAX797	9648	16 SO	80	0
MAX857	9649	8 µMAX	80	0
MAX8211	9650	8 SO	44	0
REF01	9651	8 PDIP	45	0
MAX706	9651	8 PDIP	45	0
DG381	9651	14 PDIP	77	0
MAX7129	9651	24 PDIP	77	0
MAX1635	9652	28 SSOP	77	0
MAX811	9701	4 SOT23	61	0
MAX619	9701	8 PDIP	77	0
MAX232	9701	16 PDIP	77	0
MAX1245	9701	20 PDIP	77	0
MAX148	9701	20 PDIP	77	0
MAX1245	9701	20 PDIP	77	0
MAX147	9701	20 PDIP	77	0
MAX913	9702	8 PDIP	77	0
MAX545	9702	14 PDIP	77	0
DG442	9702	16 PDIP	45	0
MAX232A	9702	16 PDIP	77	0
MAX545	9703	14 SO	45	0
MAX7219	9703	24 PDIP	77	0
MAX625	9703	24 PDIP	45	0
MAX823	9704	8 PDIP	77	0
MAX6315	9704	8 PDIP	77	0
MAX619	9706	8 PDIP	77	0
MAX779	9706	8 PDIP	76	0
MAX233A	9706	20 PDIP	77	0
MAX7219	9706	24 PDIP	77	0
MAX619	9707	8 PDIP	77	0
MAX7219	9708	24 PDIP	77	0
MAX625	9710	24 PDIP	45	0
MAX706	9711	8 PDIP	45	0
MAX8211	9712	8 SO	45	0
MAX472	9713	8 PDIP	77	0
MAX681	9713	14 PDIP	77	0
REF01	9714	8 PDIP	45	0
MAX472	9714	8 PDIP	76	0
MAX623	9715	16 PDIP	77	0
DG445	9715	16 PDIP	78	0
DG211	9715	16 PDIP	70	0
MAX4112	9716	8 SO	77	0
MAX4503	9716	8 SO	45	0
MAX232A	9716	16 PDIP	45	0
MAX233	9716	20 PDIP	77	0
MAX619	9717	8 SO	45	0
MAX232	9718	16 PDIP	45	0
MAX233A	9718	20 WSO	45	0
MAX552	9719	10 µMAX	41	0
MAX233A	9719	20 WSO	45	0
MAX551	9720	10 µMAX	42	0
REF01	9721	8 PDIP	45	0
MAX8213	9721	16 SO	45	0
MAX1647	9721	20 SSOP	45	0
MXL1013	9722	8 PDIP	77	0
MAX690	9722	8 PDIP	77	0
DG381	9722	14 PDIP	45	0
DG445	9722	16 PDIP	45	0
MAX233A	9722	20 WSO	45	0
MAX690	9723	8 PDIP	77	0
MAX471	9723	8 PDIP	77	0
MAX797	9723	16 SO	45	0
MAX233A	9723	20 WSO	45	0
MAX8863	9724	5 SOT23	40	0
MAX706	9724	8 PDIP	45	0
MAX8211	9724	8 SO	45	0
MAX232	9724	16 PDIP	77	0
MAX384	9724	18 NSO	41	0
MAX8863	9725	8 PDIP	77	0
MAX667	9725	8 SO	45	0
MAX233	9725	20 PDIP	45	0
MAX203	9725	20 WSO	45	0

TABLE 13. PRESSURE POT TEST AT 121°C/100% R.H./ 15 PSIG/168 HRS. (ALL PLASTIC PACKAGES) (*continued*)

DEVICE TYPE	DATE CODE	PKG.	SAMPLE SIZE	FAILURES
MAX211E	9725	28 SSOP	50	0
MAX667	9726	8 SO	45	0
MAX1620	9726	16 QSOP	45	0
MAX233	9726	20 PDIP	45	0
MAX6809	9727	3 SOT23	40	0
MAX232A	9727	16 PDIP	45	0
MAX1603	9727	28 SSOP	76	0
MAX4333	9729	10 µMAX	45	0
MAX232	9729	16 WSO	45	0
MAX527	9729	24 WSO	35	0
DG445	9730	16 SO	45	0
MAX232	9730	16 WSO	45	0
MAX502	9730	24 WSO	45	0
REF01	9731	8 PDIP	45	0
MAX1617	9731	16 QSOP	39	0
MAX734	9734	8 PDIP	77	0
MAX8211	9735	8 SO	45	0
MAX8211	9735	8 SO	45	0
MAX706	9736	8 PDIP	45	0
MAX667	9736	8 SO	45	0
MAX890	9736	8 SO	45	0
MAX1617	9736	16 QSOP	44	0
MX7545	9736	20 PDIP	77	0
MAX547	9736	44 PLCC	45	0
MAX811	9737	8 PDIP	45	0
MAX850	9737	8 SO	41	0
MAX798	9737	16 SO	45	0
MAX547	9737	44 PLCC	45	0
MAX232A	9739	16 PDIP	45	0
MAX232	9739	16 PDIP	45	0
MAX547	9739	44 PLCC	45	0
MAX4180	9741	6 SOT23	74	0
MAX1617	9742	16 QSOP	45	0
MAX547	9742	44 PLCC	44	0
MAX1617	9743	16 QSOP	50	0
MAX1617	9744	16 QSOP	50	0
MAX849	9745	16 SO	77	0
MAX232	9746	16 WSO	45	0
MAX707	9747	8 SO	42	0
MAX619	9748	8 SO	45	0
MAX232	9748	16 WSO	45	0
MAX734	9749	8 PDIP	77	0
MAX456	9749	40 PDIP	77	0
MAX8211	9749	8 SO	45	0
MAX708	9751	8 PDIP	45	0
MAX1617	9751	16 QSOP	50	0
DG411	9751	16 PDIP	45	0
MAX232A	9752	16 PDIP	45	0
MAX1617	9752	16 QSOP	50	0
MAX619	9801	8 SO	45	0
MAX1617	9802	16 QSOP	50	0
DG318	9803	14 PDIP	45	0
MAX843	9806	8 SO	45	0
MAX797	9807	16 SO	45	0
MAX890	9811	8 SO	45	0
MAX887	9813	8 SO	45	0
MAX707	9813	8 PDIP	45	0
MAX232	9813	16 PDIP	45	0
MAX232A	9814	16 SO	45	0
MAX6160	9815	8 SO	45	0
MAX8211	9815	8 SO	45	0
MAX1664	9821	20 TSSOP	45	0
REF02	9821	8 PDIP	45	0
MAX232A	9823	16 PDIP	45	0
MAX1664	9824	20 TSSOP	45	0
MAX887	9826	8 SO	45	0
MAX850	9827	8 SO	45	0
MX7543	9829	16 PDIP	77	0
REF02	9835	8 PDIP	45	0
MAX3081	9836	8 PDIP	45	0
MAX705	9839	8 PDIP	45	0
MAX8211	9841	8 SO	45	0
TOTALS			**7945**	**0**

TABLE 14. HAST TEST RESULTS AT 120°C/85% R.H./ BIASED, 100 HRS.

DEVICE TYPE	DATE CODE	PKG.	SAMPLE SIZE	FAILURES (HRS) 100	NOTES
MAX619	9701	8 PDIP	25	0	
MAX232	9701	16 PDIP	25	0	
MAX232A	9702	16 PDIP	25	0	
MAX823	9704	8 PDIP	25	0	
MAX233A	9706	20 PDIP	25	0	
MAX7219	9706	24 PDIP	25	0	
MAX7219	9708	24 PDIP	25	0	
MAX681	9713	14 PDIP	25	0	
MAX623	9715	16 PDIP	25	0	
DG445	9715	16 PDIP	25	0	
MAX232A	9716	16 PDIP	25	0	
MAX1603	9717	28 SSOP	25	0	
MAX1630	9717	28 SSOP	25	0	
MAX233A	9718	20 WSO	25	0	
MAX233A	9719	20 WSO	25	0	
MAX552	9719	10 µMAX	25	0	
MAX551	9720	10 µMAX	25	0	
MAX690	9722	8 PDIP	25	0	
MAX690	9723	8 PDIP	25	0	
MAX719	9723	16 SO	25	0	
MAX232	9724	16 PDIP	25	0	
MAX8863	9724	5 SOT23	25	0	
MAX8863	9725	8 PDIP	25	0	
MAX203	9725	20 WSO	25	0	
MAX232A	9727	16 PDIP	24	0	
MAX1603	9727	28 SSOP	25	0	
MAX4333	9729	10 µMAX	24	0	
MAX734	9734	8 PDIP	25	0	
MAX8211	9735	8 SO	24	0	
MAX547	9736	44 PLCC	25	0	
MX7545	9736	20 PDIP	25	0	
MAX1617	9736	16 QSOP	47	0	
MAX850	9737	8 SO	25	0	
MAX798	9737	16 SO	25	0	
MAX547	9737	44 PLCC	25	0	
MAX232A	9739	16 PDIP	25	0	
MAX232	9739	16 PDIP	25	0	
MAX547	9739	44 PLCC	25	0	
MAX768	9741	16 QSOP	25	0	
MAX547	9742	44 PLCC	25	0	
MAX1617	9742	16 QSOP	52	0	
MAX768	9743	16 QSOP	25	0	
MAX1617	9743	16 QSOP	25	0	
MAX849	9745	16 SO	25	0	
MAX8211	9749	8 SO	25	0	
MAX232A	9752	16 PDIP	25	1	Unknown
MAX619	9801	8 PDIP	45	0	
DG381	9803	14 PDIP	25	0	
MAX843	9806	8 SO	25	0	
MAX887	9811	8 SO	25	0	
MAX232A	9814	16 PDIP	25	0	
MAX6160	9815	8 SO	25	0	
MAX1664	9821	20 TSSOP	23	0	
MAX232A	9823	16 PDIP	25	0	
MAX1664	9824	20 TSSOP	25	0	
MAX807	9824	16 PDIP	25	0	
MAX3081	9836	8 PDIP	25	0	
MAX232A	9838	16 PDIP	25	0	
DG201	9839	16 PDIP	25	0	
MAX232A	9840	16 PDIP	25	0	
Totals			**1564**	**1**	

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TABLE 15. TEMPERATURE CYCLING AT -65°C TO +150°C , 1000 CYCLES
(ALL PACKAGE TYPES)

DEVICE TYPE	DATE CODE	PKG.	SAMPLE SIZE	FAILURES (CYCLES)			NOTES
				200	500	1000	
MAX846	9640	16 QSOP	77	0	0	0	
MAX8211	9650	8 SO	77	0	0	0	
REF01	9651	8 PDIP	76	0	0	0	
MAX706	9651	8 PDIP	77	0	0	0	
DG381	9651	14 PDIP	77	0	0	0	
MAX619	9701	8 PDIP	77	0	0	0	
MAX232	9701	16 PDIP	77	0	0	0	
MAX811	9701	4 SOT23	75	0	0	0	
MAX913	9702	8 PDIP	77	0	0	0	
DG442	9702	16 PDIP	77	0	0	0	
MAX232A	9702	16 PDIP	77	0	0	0	
MAX545	9702	14 PDIP	77	0	0	0	
MAX545	9703	14 SO	77	0	0	0	
MAX779	9706	8 PDIP	77	0	0	0	
MAX619	9706	8 PDIP	77	0	0	0	
MAX7219	9706	14 PDIP	77	0	0	0	
MAX619	9707	8 PDIP	77	0	0	0	
MAX7219	9708	24 PIDP	77	0	0	0	
MAX706	9711	8 PDIP	77	0	0	0	
MAX8211	9712	8 SO	77	0	0	0	
REF01	9714	8 PDIP	77	0	0	0	
DG445	9715	16 PDIP	77	0	0	0	
DG211	9715	16 PDIP	77	0	0	0	
MAX232A	9716	16 PDIP	77	0	0	0	
MAX4112	9716	8 SO	77	0	0	0	
MAX1603	9717	28 SSOP	44	0	0	0	
MAX207	9718	24 CERDIP	77	0	0	0	
MAX552	9719	10 µMAX	77	0	0	0	
MAX551	9720	10 µMAX	77	0	0	0	
REF01	9721	8 PDIP	77	0	0	0	
MAX690	9722	8 PDIP	77	0	0	0	
DG381	9722	14 PDIP	77	0	0	0	
DG445	9722	16 PDIP	77	0	0	0	
MAX690	9723	8 PDIP	77	0	0	0	
MAX232	9724	16 PDIP	77	0	0	0	
MAX8863	9724	8 PDIP	45	0	0	0	
MAX8211	9724	8 SO	77	0	0	0	
MAX706	9724	8 PDIP	77	0	0	0	
MAX719	9724	16 SO	45	0	0	0	
MAX8863	9725	5 SOT23	45	0	0	0	
MAX667	9725	8 SO	71	0	0	0	
MAX667	9726	8 SO	77	0	0	0	
MX7533	9726	16 SO	45	0	0	0	
MAX232A	9727	16 PDIP	77	0	0	0	
MAX1603	9727	28 SSOP	45	0	0	0	
MAX4333	9729	10 µMAX	77	0	0	0	
DG445	9730	16 PDIP	77	0	0	0	
REF01	9731	8 PDIP	77	0	0	0	
MX7533	9733	16 CERDIP	45	0	0	0	
MAX4333	9729	10 µMAX	77	0	0	0	
DG445	9730	16 PDIP	77	0	0	0	
REF01	9731	8 PDIP	77	0	0	0	
MX7533	9733	16 CERDIP	45	0	0	0	
MX574	9734	28 CERDIP	45	0	0	0	
MAX734	9734	8 PDIP	77	0	0	2	Unknown
MAX768	9734	16 QSOP	45	0	0	0	

DEVICE TYPE	DATE CODE	PKG.	SAMPLE SIZE	FAILURES (CYCLES)			NOTES
				200	500	1000	
MAX8211	9735	8 SO	77	0	0	0	
MAX547	9736	44 PLCC	45	0	0	0	
MX7545	9736	20 PDIP	77	0	0	0	
MAX667	9736	8 SO	45	0	0	0	
MAX890	9736	8 SO	45	0	0	0	
MAX706	9736	8 PDIP	77	0	0	0	
MAX850	9737	8 SO	45	0	0	0	
MAX798	9737	16 SO	45	0	0	0	
MAX798	9737	16 SO	77	0	0	0	
MAX811	9737	8 PDIP	77	0	0	0	
MAX547	9737	44 PLCC	45	0	0	0	
DG507	9737	28 CERDIP	77	0	0	0	
DG381	9738	14 PDIP	77	0	0	0	
MAX232A	9739	16 PDIP	76	0	0	0	
MAX232	9739	16 PDIP	77	0	0	0	
MAX547	9739	44 PLCC	45	0	0	0	
MAX232	9739	16 CERDIP	77	0	0	0	
MAX547	9742	44 PLCC	45	0	0	0	
ICM7217	9742	28 CERDIP	77	0	0	0	
MAX849	9745	16 SO	77	0	0	0	
MAX547	9746	44 PLCC	25	0	0	0	
MAX768	9746	16 QSOP	45	0	0	0	
MAX547	9749	44 PLCC	25	0	0	0	
MAX8211	9749	8 SO	77	0	0	0	
MAX708	9751	8 PDIP	77	0	0	0	
DG411	9801	16 PDIP	77	0	0	0	
DG381	9803	14 PDIP	77	0	0	0	
MAX843	9806	8 SO	45	0	0	0	
MAX797	9807	16 SO	77	0	0	0	
MAX890	9811	8 SO	45	0	0	0	
MAX887	9813	8 SO	77	0	0	0	
MAX707	9813	8 PDIP	77	0	0	0	
MAX232A	9814	16 PDIP	77	0	0	0	
MAX8211	9815	8 SO	77	0	0	0	
MAX1664	9821	20 TSSOP	77	0	0	0	
REF02	9821	8 PDIP	77	0	0	0	
MAX232A	9823	16 PDIP	77	0	0	0	
MAX1614	9824	20 TSSOP	77	0	0	0	
MAX807	9824	16 PDIP	77	0	0	0	
MAX705	9826	8 PDIP	77	0	0	0	
MAX528	9826	20 PDIP	77	0	0	0	
MAX887	9827	8 SO	77	0	0	0	
MAX850	9827	8 SO	77	0	0	0	
MX7543	9829	16 PDIP	77	0	0	0	
REF02	9835	8 PDIP	77	0	0	0	
MAX691A	9836	16 SO	77	0	0	0	
MAX3081	9836	8 PDIP	77	0	0	0	
MAX232A	9838	16 PDIP	77	0	0	0	
MAX705	9839	8 PDIP	77	0	0	0	
DG201	9839	16 PDIP	77	0	0	0	
MAX232A	9840	16 PDIP	77	0	0	0	
MAX8211	9841	8 SO	77	0	0	0	
Totals			**7343**	**0**	**0**	**0**	

TABLE 16. HIGH-TEMPERATURE STORAGE LIFE TEST AT 150°C/1000 HRS. (ALL PACKAGE TYPES)

DEVICE TYPE	DATE CODE	PKG.	SAMPLE SIZE	FAILURES (HRS)		
				168	500	1000
MAX8211	9650	8 SO	45	0	0	0
REF01	9651	8 PDIP	45	0	0	0
MAX706	9651	8 PDIP	42	0	0	0
DG381	9651	14 PDIP	45	0	0	0
MAX619	9701	8 PDIP	77	0	0	0
MAX232	9701	16 PDIP	45	0	0	0
MAX913	9702	8 PDIP	45	0	0	0
DG442	9702	16 PDIP	45	0	0	0
MAX232A	9702	16 PDIP	45	0	0	0
MAX779	9706	8 PDIP	44	0	0	0
MAX619	9706	8 PDIP	45	0	0	0
MAX7219	9706	24 PDIP	45	0	0	0
MAX619	9707	8 PDIP	45	0	0	0
MAX706	9711	8 PDIP	45	0	0	0
MAX8211	9712	8 SO	45	0	0	0
REF01	9714	8 PDIP	45	0	0	0
DG445	9715	16 PDIP	45	0	0	0
DG211	9715	16 PDIP	45	0	0	0
MAX232A	9716	16 PDIP	45	0	0	0
MAX4112	9716	8 SO	45	0	0	0
MAX1603	9717	28 SSOP	45	0	0	0
MAX207	9718	24 CERDIP	45	0	0	0
MAX552	9719	10 µMAX	45	0	0	0
MAX551	9720	10 µMAX	44	0	0	0
REF01	9721	8 PDIP	45	0	0	0
MAX690	9722	8 PDIP	45	0	0	0
MAX8211	9735	8 SO	45	0	0	0
MX574	9735	28 CERDIP	44	0	0	0
MAX8211	9735	8 SO	45	0	0	0
MAX547	9736	44 PLCC	45	0	0	0
MX7545	9736	20 PDIP	45	0	0	0
MAX667	9736	8 SO	45	0	0	0
MAX706	9736	8 PDIP	45	0	0	0
MAX850	9737	8 SO	45	0	0	0
MAX798	9737	16 SO	44	0	0	0
MAX798	9737	16 SO	45	0	0	0
MAX811	9737	8 PDIP	45	0	0	0
MAX547	9737	44 PLCC	10	0	0	0
DG507	9737	28 CERDIP	45	0	0	0
DG381	9738	14 PDIP	77	0	0	0
MAX232A	9739	16 PDIP	77	0	0	0
MAX232	9739	16 PDIP	77	0	0	0
MAX547	9739	44 PLCC	45	0	0	0
MAX768	9741	16 QSOP	45	0	0	0
MAX547	9742	44 PLCC	45	0	0	0
MAX1617	9742	16 QSOP	100	0	0	0
ICM7217	9742	28 CERDIP	45	0	0	0
MAX768	9743	16 QSOP	45	0	0	0
MAX1617	9743	16 QSOP	100	0	0	0
MAX1632	9744	28 SSOP	45	0	0	0
MAX1617	9744	16 QSOP	100	0	0	0
MAX849	9745	16 SO	45	0	0	0
MAX768	9750	16 QSOP	45	0	0	0
MAX8211	9749	8 SO	77	0	0	0
MAX708	9751	8 PDIP	45	0	0	0
DG411	9751	16 PDIP	77	0	0	0
MAX232A	9752	16 PDIP	77	0	0	0
MAX619	9801	8 PDIP	45	0	0	0
DG381	9803	14 PDIP	77	0	0	0
MAX843	9806	8 SO	45	0	0	0
MAX890	9811	8 SO	45	0	0	0
MAX887	9813	8 SO	45	0	0	0
MAX707	9813	8 PDIP	45	0	0	0
MAX232	9813	16 PDIP	45	0	0	0
MAX232A	9814	16 PDIP	45	0	0	0
MAX6160	9815	8 SO	45	0	0	0
MAX8211	9815	8 SO	45	0	0	0
MAX1664	9821	20 TSSOP	45	0	0	0
REF02	9821	8 PDIP	45	0	0	0
MAX232A	9823	16 PDIP	45	0	0	0
MAX1664	9824	20 TSSOP	45	0	0	0
MAX705	9826	8 PDIP	45	0	0	0
MAX528	9826	20 PDIP	77	0	0	0
MAX887	9827	8 SO	45	0	0	0
MAX850	9827	8 SO	45	0	0	0
MX7543	9829	16 PDIP	77	0	0	0
REF02	9835	8 PDIP	45	0	0	0
MAX3081	9836	8 PDIP	45	0	0	0
MAX232A	9838	16 PDIP	77	0	0	0
DG201	9839	16 PDIP	77	0	0	0
MAX705	9839	8 PDIP	77	0	0	0
MAX232A	9840	16 PDIP	45	0	0	0
MAX8211	9841	8 SO	77	0	0	0
Totals			**5148**	**0**	**0**	**0**

TABLE 17. HYBRID PRODUCT LIFE TEST AT 135°C/1000 HRS.

DEVICE TYPE	DATE CODE	PKG.	SAMPLE SIZE	FAILURES (HRS)		
				192	500	1000
LH0101	9706	TO3	80	0	0	0
MAX1480	9712	18 PDIP	77	0	0	0
MAX681	9713	14 PDIP	77	0	0	0
MAX623	9715	16 PDIP	77	0	0	0
MAX203	9725	20 WSO	77	0	0	0
MAX3089	9750	14 PDIP	76	0	0	0
MAX681	9818	14 PDIP	77	0	0	0
LH0033	9821	12 TO	30	0	0	0
LH101	9824	8 TO	45	0	0	0
LH0033	9824	12 TO	45	0	0	0
Totals			**661**	**0**	**0**	**0**

TABLE 18. HYBRID PRODUCTS TEMPERATURE CYCLING AT -65°C to +150°C, 1000 CYCLES

DEVICE TYPE	DATE CODE	PKG.	SAMPLE SIZE	FAILURES (CYCLES)		
				192	500	1000
MAX625	9703	24 PDIP	43	0	0	0
MAX681	9713	14 PDIP	77	0	0	0
MAX623	9715	16 PDIP	77	0	0	0
MAX203	9725	20 WSO	77	0	0	0
MAX681	9818	14 PDIP	45	0	0	0
LH101	9824	8 TO	40	0	0	0
LH0033	9824	12 TO	35	0	0	0
Totals			**394**	**0**	**0**	**0**

Product Reliability Report

Appendix 1: Acceleration Factor Calculation

Definition of Terms

The thermal acceleration factor represents the temperature enhancement of the failure rate, and expresses the ratio of the failure rates at two temperatures. The Arrhenius equation is used to calculate the acceleration factor, given as A below:

$$A = \exp [(E_a / k_B) \times \{ (1/T_u) - (1/T_s) \}]$$

where:

E_a = the activation energy in eV

k_B = the Boltzmann constant, 8.617×10^{-5} eV/K

T_u = use temperature, in degrees Kelvin

T_S = stress test temperature in degrees Kelvin

In using the formula above, we must know the activation energy, Ea, which may be accomplished in one of two ways.

Use Existing Activation Energy Information

The first method is to use an existing estimate of the activation energy. Activation energies for many failure mechanisms have been tabulated and published in the technical literature. The dominant failure mechanisms have activation energies in the range of 0.7eV to 1.2eV. We have chosen 0.8eV for the purposes of calculating the acceleration factors used in this report. Many failure processes have larger activation energies.

Measure the Activation Energy

The second method of determining an activation energy is empirical. The failure rates of two groups of devices are tested at different temperatures, and the ratio A of their failure rates is calculated. An example is shown below:

Group 1 = 60/1000 failures after 100 hrs. of operation at 150°C.

Group 2 = 15/1000 failures after 100 hrs. of operation at 125°C.

The acceleration factor between these two temperatures is, therefore, A = 60/15 = 4. The activation energy Ea is given by:

$$E_a = k_B \times \ln[A] / \{ (1/T_u) - (1/T_S) \} = 0.8eV$$

where:

E_a = the unknown activation energy

T_u = 125°C + 273°C = 398°K

T_S = 150°C + 273°C = 423°K

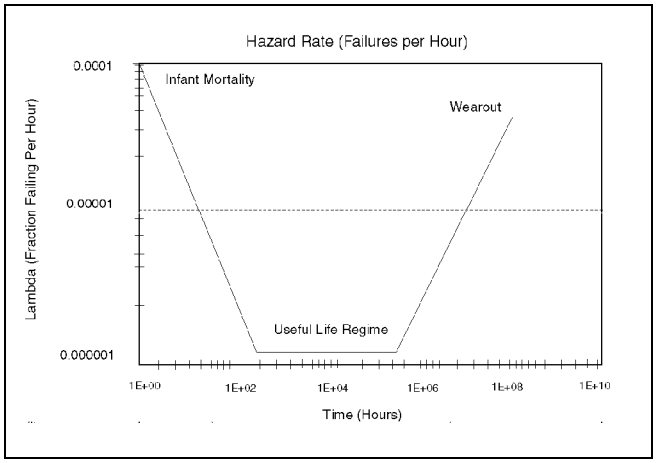
ln = the natural logarithm function

The other terms are as defined above.

Assuming that this activation energy represents the dominant failure mechanism of the device under consideration, it may then be used to determine the acceleration factor between any two temperatures. For example, to find out the acceleration factor between 150°C and 70°C, substitute T_u = 70°C + 273°C = 343°K and T_S = 150°C + 273°C = 423°K. Acceleration Factor = 165.

Appendix 2: Determining Failure Rates

In describing semiconductor reliability, we must first define a few basic terms[1]. We define the total fraction of failures versus time to be the cumulative distribution function F(t). The survivor function S(t) is 1 - F(t). The instantaneous failure rate f(t) is the time derivative dF(t)/dt. Finally, the hazard rate $\lambda(t)$ is the instantaneous failure rate f(t) normalized to the surviving population S(t); $\lambda(t) = f(t) / S(t)$.



It is the hazard rate, plotted versus time t, that shows the characteristic bathtub curve behavior shown above. The three major regimes of this curve are the infant mortality regime, the useful life regime, and the wearout regime. We discuss each regime separately below.

Initially, the hazard rate is seen to decrease steadily over time, which defines the infant mortality phase.

[1] *In this discussion, we employ the terminology of semiconductor reliability found in D.J. Klinger, Y. Nakada, and M. A. Menendez, AT&T Reliability Manual, Van Nostrand Reinhold, New York,1990.*

In the infant mortality regime, the hazard rate commonly follows a Weibull function, given by:

$$\lambda(t) = \lambda o \times t^{-\alpha}$$

where λo and α are constant parameters. Maxim tests the infant mortality failure rate with short (12 to 24 hour) burn-in tests, which are shown in Table 4 of this report.

The infant mortality period is found to eventually give way to a rather constant hazard rate, in the "useful life regime." This period is still described by the Weibull function, with the parameter $\alpha = 0$. The constant hazard rate function is also known as the "exponential distribution." During the useful life period, the Mean Time to Failure (MTTF), which is the average time for a failure to occur, is simply equal to the inverse of the hazard rate. For example, assume a company tests 1000 units to 1000 hours. The total device-hours accrued would be 1,000,000 device-hours. If two units were found to be failures, the MTTF would be:

MTTF= Total Device Hours/Total Failures = 1,000,000 hrs./2 = 500,000 hrs.
and the hazard rate (λ) is:

$$\lambda = 1/MTTF = 1/500,000 = 0.000002$$

If this number is multiplied by 10^5 the failure rate in terms of percent per 1000 hours is obtained; i.e., 0.2% per 1000 hours.

As failure rates are usually so small, they are commonly describe in terms of the FIT rate. The term FIT is short for Failure-in-Time, and specifically, this is defined to be the number of failures per billion device-hours. Thus, the FIT rate is obtained by multiplying the Failure Rate per hour by 10^9:

$$\lambda \text{ in FITs} = \lambda \text{ per hr.} \times 10^9$$

Using the above example:

$$\lambda \text{ in FITs} = 0.000002/10^{-9} = 2,000 \text{ FITs}$$

The FIT rate is, therefore, shorthand for the number of units predicted to fail in a billion (10^9) device-hours at the specified temperature.

Calculating Failure Rates and FITs

The failure rate can be determined from the following four variables:

A = the number of failures observed after test

B = the number of hours the test was run

C = the number of devices used in the test

D = the temperature acceleration factor (see Appendix 1)

Using data in Table 3, a failure rate at 25°C can now be calculated:

A = 27

B = 192

C = 12,565

D = 9822 (assuming Ea = 0.8eV, and a test temperature of 150°C)

Substituting:

$$\lambda = 27 / (192 \times 12,565 \times 9822) = 1.14 \times 10^{-9} \text{ per hr.}$$

Expressing this in terms of the FIT rate:

$$\lambda = 1.14 \text{ FITs}$$

To determine the FIT rate at a new temperature, the acceleration factor (D) must be recalculated from the Arrhenius equation given in Appendix 1.

Including Statistical Effects in the FIT Calculation

Because the number of failures observed from a reliability test sample is usually small, there is a statistical likelihood that the actual failure rate may be higher or lower than the raw value calculated above. Therefore, we can calculate the failure rate for any given required confidence level. Common confidence levels are 60% or 90%. We are usually concerned with determining the upper confidence level or "UCL." The 60% UCL expresses the highest failure rate that would be found 60% of the time, based on a random sample from the Chi-square distribution.

The failure rate calculation, including a confidence level, is determined as follows:

$$\lambda = \chi^2 / 2DH$$

where:

χ^2 = the Chi square value

2DH = 2 times the total device hours = $2 \times (B \times C \times D)$

The Chi-square distribution may be found from standard statistical tables. There are two parameters of the Chi-square distribution, the degrees of freedom (df) and the confidence level. The degrees of freedom is 2 × (failures + 1). In the example above, the number of degrees of freedom is df = 2 × (27 + 1) = 56. If we desire a 60% UCL, the tabu-

lated Chi-square value found under the values of (1 - 60%) = 0.40 and 56 degrees of freedom is 57.64. Therefore, the failure rate found using a 60% confidence level is:

$$\lambda = 57.64 / (4.74 \times 10^{10}) = 1.22 \times 10^{-9}$$

or:

$$\lambda = 1.22 \text{ FITs}$$

Referring to Table 3, one can see that for Maxim's products, to a 60% confidence level, we estimate that 1.22 units will fail per billion (10^9) device-hours of operation at 25°C.

Appendix 3:
Process Information

This section defines the layer-by-layer construction steps used in the fabrication of each process.

(1) SMG (Refer to Figure 1)

Layer	Description	Dimension
1	P-Well Diffusion	10µm
2	P+ Diffusion	2µm
3	N+ Diffusion	2µm
4	Gate-Oxide Growth	900Å
5	Threshold Implant	
6	Contact Etch	
7	Metallization	1µm (Al, Si-1%)
8	Passivation	0.8µm (Si_3N_4 over SiO_2)

(2) MV1 (Refer to Figure 2)

Layer	Description	Dimension
0	Buried Layer	10µm
1	EPI Deposit	19µm
2	P-Well Diffusion	10µm
3	P+ Diffusion	3µm
4	N+ Diffusion	3µm
5	Gate-Oxide Growth	1975Å
6	Threshold Implant	
7	Contact	
8	Metallization	1µm (Al, Si-1%)
9	Passivation	0.8µm (Si_3N_4 over SiO_2)

(3) MV2 (Refer to Figure 3)

Layer	Description	Dimension
1	Buried Layer	24.0µm
2	P Well	10.0µm
3	P+ Diffusion	1.5µm
4	N+ Diffusion	1.5µm
5	Gate-Oxide Growth	1000Å
6	P-Ch Threshold Adjust	
7	Polysilicon	4500Å
8	NLDD	
9	PLDD	
10	N+ Ohmic	
11	Contact	
12	Metallization	1.0µm
13	Passivation	0.8µm

(4) SG3 (Refer to Figure 4)

Layer	Description	Dimension
1	P Well	6.0µm
2	PNP Base	
3	Zener Implant	
4	Active Area	1.5µm
5	P Guard	
6	N Guard	
7	P-Ch Threshold Adjust	
8	Poly 2	7000Å
9	Poly 1	4000Å
10	N+ Block	
11	P+ Select	
12	Thin Film	
13	CrSi Contact	
14	Contact	
15	Metallization	1.0µm
16	Passivation	0.8µm (Si_3N_4 over SiO_2)

(5) SG5 (Refer to Figure 5)

Layer	Description	Dimension
1	P-Well Diffusion	8µm
2	PNP Base Drive	
3	Zener Implant	
4	Active Area/Field Ox	1µm
5	N Guard	
6	P Guard	
7	Threshold Adjust	
8	Gate-Oxide Growth	750Å
9	Polysilicon 1	4400Å
10	Cap Oxide	1000Å
11	Polysilicon 2	4400Å
12	N+ Implant (Source/Drain)	
13	P+ Implant (Source/Drain)	
14	Chrome/Si Thin-Film Deposit	
15	Contact	
16	Metallization	1µm
17	Passivation	0.8µm (Si_3N_4 over SiO_2)

(6) SG1.2 (Refer to Figure 6)

Layer	Description	Dimension
0	Mark Layer on P Substrate	
1	N+ Buried Layer	4µm
2	P+ Buried Layer	6µm
3	P Well	2.8µm
4	NPN Base	
5	PNP Base	
6	Active Area	
7	P Guard	
8	N Guard	
9	Gate-Oxide Growth	230Å
10	Poly 1	4200Å
11	Poly 2	4200Å
12	NMOS LDD	
13	N+ Implant (Source/Drain)	0.3µm
14	P+ Implant (Source/Drain)	0.3µm
15	Thin Film (Chrome/Si)	
16	Contact	
17	TF Contact	
18	Metal 1	6000Å
19	Metal 1 Options	
20	Via	
21	Metal 2	1.0µm
22	Passivation	8000Å

(7) BIP (Refer to Figure 7)

Layer	Description	Dimension
1	N+ Buried Layer	4.5µm
2	P+ Isolation	20µm
3	P Base	3µm
4	N+ Emitter	2.5µm
5	Capacitor	1500Å
6	Contact Etch	
7	Aluminum	11kÅ (Al, Si-1%)
8	Passivation	8kÅ (Si_3N_4 over SiO_2)