Technical Compliance Statement

(Completed statement must be uploaded during online bid submission)

Sr. No.	Specifications	Values / Description *(to be filled as per technical specification of the item offered by the bidder)*
	FPGA Evaluation Board having: -	
1	FPGA device should be a programmable SoC with ➢ Dual core ARM® Cortex-A9 based processor or equivalent ➢ At least 85K DSP slices Logic Cells ➢ At least 4.9 Mb Block RAM ➢ At least 220 DSP Slices ➢ At least 200 High Range I/O with support for I/O voltage from 1.2V to 3.3V	
2	Memory: ➢ 1 GB DDR3 or more ➢ 128 Mb Quad SPI flash memory or more	
3	Clock Sources: ➢ Fixed 200 MHz LVDS oscillator or better ➢ I^2C programmable LVDS oscillator	
4	I/O Ports / peripherals: ➢ At least Two VITA 57.1 FMC LPC connectors ➢ USB 2.0 transceiver ➢ Secure Digital (SD) connector ➢ At least one Ethernet PHY RGMII interface with RJ-45 connector ➢ USB-to-UART bridge ➢ At least two programmable logic (PL) user pushbuttons ➢ At least two programmable DIP switch (2-pole) ➢ At least Eight user programmable LEDs ➢ At least one Dual row and one Single row Pmod GPIO header ➢ At least one HDMI output port	
5	Other Features ➢ Status LEDs for Ethernet status, Power good, FPGA INIT and FPGA DONE ➢ RTC (real time clock) ➢ HDMI codec	
6	➢ Power On/Off Switch ➢ 12V @ 5A AC/DC regulator or similar	
7	Programming/ Configuration Options: ➢ Quad SPI flash memory ➢ USB JTAG configuration port ➢ Platform cable header JTAG configuration port	
8	FPGA programming and design Software needs to be provided	
9	Power supply adapter and cable, SD card, Programming cable should be provided	
10	1 year standard warranty	
	DAC Module with FMC Interface	
1	Digital to Analog Conversion (DAC) Evaluation Board	
2	Data Update Rate of 2.5 GSPS or more	
3	DAC Resolution of 14 Bits or more	
4	DAC Accuracy: ➢ DNL = ±2.5 LSB or better ➢ INL = ±2.0 LSB or better	
5	Analog Output ➢ Programmable full scale output current ➢ Output Capacitance 1 pF or lesser ➢ Output Compliance Range in −1.0V to +1.0 V or better ➢ Bandwidth of 1.25 GHz or better	
6	Operating Supply Voltage of 3.3 V	

7	Clock Selection Provision for external clock and internal oscillator	
8	FPGA Interface with FMC Connector (LPC)	
9	Reference Design for the offered FPGA board should be provided.	
10.	Board support packages and drivers should be available.	
11	1 year standard warranty.	
	ADC Module with FMC Interface	
1	Analog to Digital Conversion (ADC) Evaluation Board	
2	Sampling Rate of 250 Msps or more	
3	2.5 Vp-p differential analog input	
4	At least 1 (one) No. of input channels	
5	ADC resolution of 16 Bits or more	
6	ADC Linearity with DNL = ±0.5 LSB and INL = ±3.5 LSB or better	
7	Provision for external clock and internal oscillator	
8	Operating Supply Voltage of 3.3 V	
9	FPGA Interface with FMC Connector (LPC)	
10.	Customizable with SPI interface for setup and control.	
11	Operating Temperature of -40 °C to 85 °C	
12	Reference Design for the offered FPGA board should be provided.	
13	Board support packages and drivers should be available.	
14	1 year standard warranty	

Bidder's signature and stamp