Final Year Project Proposal 1

Project Title:
Electromigration reliability study of metallic nanowires

Supervisor:
Assoc. Prof. Gan Chee Lip

Graduate Mentor:
Ms Chun Shu Rong

Description:
As scaling of devices continues, a 50 μm solder bump is experiencing a high current density in the order of 10^4 A/cm^2. This poses serious reliability problem in terms of electromigration for future devices. Thus, arrays of metallic nanowires have been proposed as an alternative to solder bump interconnection. An electromigration statistical study of a bottom-up fabricated single nanowire will be done so as to model the nanowire arrays electromigration behavior.

Methodology:
Metallic nanowires can be fabricated via electrodeposition through porous alumina template. Free standing nanowires can be achieved by removal of the template and liberation in a bottle of solvent. This is followed by alignment of single nanowire between two electrode pads using the dielectrophoresis method. After which, platinum will be use to connect to two other electrode pads for four-point electrical measurement and electromigration test using wafer-level and package-level testing.

Equipment:
Anodization setup (NTU)
Potentiostat (NTU)
Scanning Electron Microscopy (NTU)
Function generator (NTU)
Probe Station (NTU)

Remarks:
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Final Year Project Proposal 2

Project Title:
Electrical characterization of low temperature bonding via copper nanowires for 3D ICs

Supervisor:
Assoc. Prof. Gan Chee Lip

Graduate Mentor:
Ms Chun Shu Rong

Description:
Three-dimensional (3D) integration is known to be a promising solution to scaling issues in CMOS circuits. It enables improvements in integrated circuits (ICs) performance, power consumption, system functionality and form factor. Wafer or chip bonding is an enabling technology for fabrication of 3D ICs and low temperature bonding is desired for compatibility with back-end-of-line processing conditions in order not to affect the device performance. Hence, it is necessary to research on ways to bring down the bonding temperature effectively.

It has been well understood that the surface melting point of material decreases as the surface to volume ratio increases. This characteristic can be applied to lower down the bonding temperature by changing the copper film with copper nanowires. To successfully integrate nanowires into the bonding system, characterization on the nanowires bonding needs to be investigated. In this project, the focus will be on contact resistance measurement of copper nanowires bonding and the effect of decreasing nanowire diameters.

Methodology:
First, the nanoporous alumina templates are fabricated using a two-step anodization method. Second, copper nanowires are grown through the template using electrodeposition method. Finally, the template will be etched away, leaving the nanowires standing on the substrate/chip. Two chips are then bonded at low temperature. Electrical characterization is done using the probe station while SEM/XRD is needed to characterize the fabricated nanowires.

Equipment:
Anodization equipment (NTU)
Potentiostat (NTU)
Furnace for bonding (NTU)
Probe station (NTU)
SEM/XRD (NTU)

Remarks:
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Final Year Project Proposal 3

Project Title:
Fabrication and characterization of copper nanowires-solder interconnection

Supervisor:
Assoc. Prof. Gan Chee Lip

Graduate Mentor:
Ms Ng Mei Zhen

Description:
Copper-to-copper bonding has been investigated as a solution for three-dimensional (3D) integration. Copper nanowires have been further studied to lower the bonding temperature required. Although it gives the best electrical properties, the bond strength is typically weaker than films. Thus to further improve the mechanical strength and thus reliability, using solders to bond the copper nanowires is envisioned to improve the properties.

Methodology:
First, the nanoporous alumina templates are fabricated using a two-step anodization method. Second, copper nanowires are grown through the template using electrodeposition method. Finally, the template will be etched away, leaving the nanowires standing on the substrate/chip. Solder will be sputtered deposited on another chip. The two chips are then bonded at different temperatures. Mechanical, structural and electrical characterizations are then carried out using shear test, SEM/XRD and electrical probe station respectively.

Equipment:
Anodization equipment (NTU)
Potentiostat (NTU)
Furnace for bonding (NTU)
Probe station (NTU)
SEM/XRD (NTU)
Shear tester (Simtech)

Remarks:
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Final Year Project Proposal 4

Project Title:
Graphite oxide/polymer nanocomposite film as gate insulators

Supervisor:
Assoc. Prof. Gan Chee Lip

Graduate Mentor:
Mr Han Xuanding

Description:
Graphite oxide is a derivative of graphene, where the basal planes and edges are attached with hydrophilic oxygen functional groups, leading to the ease of dispersion in polar solvents. This group of material is attractive for fabrication of low cost electronics on large area, flexible substrate by printing techniques. In this project, graphite oxide/polymer nanocomposite films will be studied for application as gate insulators.

Methodology:
MOS structure will be fabricated with the graphite oxide/polymer nanocomposite as the insulator film. Electrical characterization such as I-V, breakdown voltage and leakage currents, will be performed to investigate the performance of the insulator film.

Equipment:
Contact Angle Measurement (NTU)
FTIR (NTU)
Probe Station (NTU)

Remarks:
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Final Year Project Proposal 5

Project Title:
Electrical characterization of copper/low-k dielectrics test structures

Supervisor:
Assoc. Prof. Gan Chee Lip

Graduate Mentor:
Ms Ong Ran Xing

Description:
Low-k dielectric such as carbon doped silicon oxide and copper are being used to replace silicon dioxide and aluminum metallization to reduce resistance-capacitance (RC) delays. SiOC has weaker thermomechanical properties than SiO_2, such as lower elastic moduli, hardness and interfacial adhesion. The SiOC may have difficulty withstanding the thermal and mechanical stresses of packaging and assembly, hence the need to evaluate the long-term interconnect dielectric reliability. The objective of this project is to study the failure mechanism of the Cu/low k interconnect system.

Methodology:
To perform physical and electrical failure analysis on conventional test structures and non-conventional small area tests structures. Main focus will be on the voltage ramp test to understand the conduction mechanism. Student will be conducting test for different ramp rates at various temperatures.

Equipment:
Probe Station (NTU)
Scanning Electron Microscopy (NTU)

Remarks:
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Final Year Project Proposal 6

Project Title:
Characterization on copper protrusion on Cu-filled through silicon vias (TSVs) after annealing

Supervisor:
Assoc. Prof. Gan Chee Lip

Graduate Mentor:
Mr Wahyuaji Narottama Putra

Description:
Three-dimensional integrated circuit (3DIC) is getting more attention in the research community. The reliability of Cu-filled through silicon vias (Cu TSVs) is essential for commercial high-volume manufacturing. When annealed, the copper TSVs inside a silicon device receive high stress because of the large coefficient of thermal expansion (CTE) mismatch between copper and silicon. This stress may cause a pumping phenomenon in which the copper is forced out of blind TSVs to form a protrusion. Second annealing, on the other hand, has no effect on additional protrusion. This experiment will give better understanding by comparing the grain size on the TSVs between first and second annealing.

Methodology:
TSVs will be annealed twice at 400°C. These TSVs will be characterized by using AFM to measure the protrusion height, XRD and SEM to see the grain size. For comparison purpose, same characterization will be done for un-annealed TSVs and 400°C annealed TSVs.

Equipment:
Oven (NTU)
Mechanical Polisher (NTU)
X-ray Diffraction (NTU)
Scanning Electron Microscope (NTU)
Atomic Force Micrsocope (NTU)

Remarks:
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Final Year Project Proposal 7

Project Title:
Al_2O_3 Ceramics substrate fabrication and characterization for high pressure and temperature electronics

Supervisor:
Assoc. Prof. Gan Chee Lip

Graduate Mentor:
Dr I Made Riko

Description:
Increasing fuel demand and ever scarcity of natural resources such as oil, had driven efforts to find new oil reserve deep in earth mantel. Deep earth exploration requires a much more reliable instrumentation and sensors that can survive extreme pressure and temperature such as 2000 atm and 300^{o}C, respectively. Ceramics had been identified as suitable materials that could give reasonable protection for sensitive electronic device from extreme environment.

In this project we will focus on understanding and establishing methodology to fabricate relatively thin ceramics substrates by tape casting method. A comparison to commercially obtained ceramics substrate will be used to evaluate the relative quality of the fabricated substrate in term of mechanical and electrical properties.

Methodology:
Fabrication of ceramics substrate by tape casting method from chemical slurries and sintering. Characterization of substrate through thermal conductivity, coefficient of thermal expansion, mechanical strength.

Equipment:
Tape Casting Equipment (NTU)
Sintering Furnace (NTU)
Probe station (NTU)
SEM/EDX (NTU)

Remarks:
As this is a new project, students with independent abilities to research on the topic and plan the experiments will be preferred. This project will be done in parallel with project 8.

Final Year Project Proposal 8

Project Title:
AlN Ceramics substrate fabrication and characterization for high pressure and temperature electronics

Supervisor:
Assoc. Prof. Gan Chee Lip

Graduate Mentor:
Dr I Made Riko

Description:
Increasing fuel demand and ever scarcity of natural resources such as oil, had driven efforts to find new oil reserve deep in earth mantel. Deep earth exploration requires a much more reliable instrumentation and sensors that can survive extreme pressure and temperature such as 2000 atm and 300^{o}C, respectively. Ceramics had been identified as suitable materials that could give reasonable protection for sensitive electronic device from extreme environment.

In this project we will focus on understanding and establishing methodology to fabricate relatively thin ceramics substrates by tape casting method. A comparison to commercially obtained ceramics substrate will be used to evaluate the relative quality of the fabricated substrate in term of mechanical and electrical properties.

Methodology:
Fabrication of ceramics substrate by tape casting method from chemical slurries and sintering. Characterization of substrate through thermal conductivity, coefficient of thermal expansion, mechanical strength.

Equipment:
Tape Casting Equipment (NTU)
Sintering Furnace (NTU)
Probe station (NTU)
SEM/EDX (NTU)

Remarks:
As this is a new project, students with independent abilities to research on the topic and plan the experiments will be preferred. This project will be done in parallel with project 7.

Final Year Project Proposal 9

Project Title: Hermetic sealing of MEMS sensors for high temperature electronics

Supervisor:
Assoc. Prof. Gan Chee Lip

Co-Supervisor:
Dr Vivek Chidambaram (Institute of Microelectronics, A*STAR)

Description:
High-temperature electronics (HTE) has emerged as a strategic technology for many key industrial sectors and in particular the oil and gas industry. HTE are important for measurement during oil well drilling and for production management over the life of the well. MEMS sensors that are currently being used include temperature, pressure, radiation, acoustic, resistivity and inclination. These MEMS sensors are required to perform measurements with respect to rotation and vibration, soil conditions, pressure and radio activity. As sensors and the corresponding electronics for logging while drilling (LWD) applications are mounted inside the drilling head, they are exposed to high temperature, high pressure, vibration and corrosive liquid/gases. Practically, all MEMS sensors are adversely affected by such harsh environments. Thus, in packaging MEMS sensors in particular for LWD tools, hermetic sealing is indispensable in order to ensure their reliable operation and also to provide protection during fabrication.

Metallic hermetic sealing is now widely being used for MEMS packaging due to its slow permeability rate. In the present work, Al-Ge and Pt-In systems will be envisaged for hermetic sealing application. Al-Ge system was chosen since both these metals are CMOS compatible. CMOS compatible MEMS packaging is generally preferred since it facilitates the integration of MEMS devices with driving, controlling and signal processing electronics and thereby, improves performance and also lowers manufacturing costs. Pt-In system was also selected for this investigation since among all the systems that are being vied for diffusion soldering, it has the highest remelting temperature (894°C) which is desired by both the oil and gas exploration industry and the aerospace industry.

Methodology:
The interfacial reaction and the bonding quality of the Al-Ge eutectic bonding and the Pt-In transient liquid phase bonding (TLP) will be studied and evaluated. The optimization of the bonding parameters for both the Al-Ge eutectic bonding as well as the Pt-In TLP bonding will be executed. Microstructure characterization will be performed using advance microscopy techniques. Reliability analysis will be performed using high-temperature storage, high-humidity storage, pressure cooker test, hemeticity test and shear strength measurements.

Equipment:
Field Emission Scanning Electron Microscope, Focused Ion Beam, Scanning Acoustic microscope .
Class 100 clean room processes like sputtering, evaporation, lithography, dry and wet etching

Remarks:
The student has to spend majority of his/her time in IME. This project is a joint collaborative work between IME and MSE.

Final Year Project Proposal 10

Project Title:
Characterization of differential dual spin valve for future magnetic recording

Supervisor:
Assoc. Prof. Gan Chee Lip

Co-Supervisor:
Dr Han Guchang (Data Storage Institute, A*STAR)

Description:
Differential dual Spin valve (DDSV) is one of the most promising candidates for future magnetic readers in hard-disk-drive application. DDSV device is featured on high sensitivity, large intrinsic signal and excellent linear response. However, there are some problems, such as magnetization canting of the pinning layer. In this project, student will learn the technique to characterize DDSV device with different configurations. Working with the mentor, student will explore the mechanism of DDSV sensors and understand how a DDSV works.

Methodology:
DDSV characterization will be conducted on an rf probe station, equipped with magnetic field, current source meter and voltage meter. DDSV device with different configuration and dimensions will be investigated to explore mechanism of the magnetization instability.

Equipment:
RF probe station (DSI)
Magnetic Vacuum Annealing Oven (DSI)
VSM (DSI)
Nanovoltimenter (DSI)

Remarks:
The student has to spend majority of his/her time in DSI.

Final Year Project Proposal 11

Project Title:
Cu metallization and dielectric removal for failure analysis of ICs

Supervisor:
Assoc. Prof. Gan Chee Lip

Graduate Mentors:
Dr Liu Qing
Ms Katherine Kor

Description:
In recent years, even though a defect is well understood electrically, an image of the anomaly is needed to verify the defect location. However, ICs have more than one layer. It is impossible to view the many types of defects without first removing the overlying layers. In some cases, the removal of one layer can act as an *in-situ* decoration of another layer, masking the defect. In this situation, proper removal method is required.

In this project, a 65 nm Cu chip will be studied. Different Cu metallization removal methods will be investigated, such as mechanical etching by polishing, chemical etching and dry etching. Meanwhile, inter metal dielectric removal techniques will be investigated as well. The main focus is to avoid the damage to the underlying layers when removing the current layer.

Methodology:
FIB will be used to study the material information and thicknesses of the layer stacks of the 65 nm Cu chip. The Cu chip will be delayered by different techniques after that. Optical images of the Cu chip will be captured during the delayering process. Meanwhile, SEM with EDX is required to verify the materials and morphology as well.

Equipment:
SEM (NTU)
Polisher (NTU)
RIE (NTU)

Remarks:
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Final Year Project Proposal 12

Project Title:
Floating Gate Memory Sample Preparation of Sub-Micron Technology Node ICs

Supervisor:
Assoc. Prof. Gan Chee Lip

Graduate Mentors:
Dr Andrew Chang

Description:
In many of today's electronic devices, flash memory has played a vital role and shaped modern life as we know it. The reliability and retention of data stored in such Non Volatile Memory (NVM) are key issues for manufacturers of such microelectronic devices. In this project, sub-micron technology node EEPROM (Electrically Erasable Programmable Read Only Memory) microchips will be studied. Traditional front-side layer by layer deprocessing to uniformly arrive at the ONO (oxide nitride oxide) level of the floating gate transistor array, where the charges are stored, will be attempted. Different passivation, metallization and ILD (inter-metal dielectric) removal methods will be investigated, such as mechanical etching by polishing, chemical etching and dry etching.

Methodology:
SEM/FIB will be used to study the material information and thicknesses of the layer stacks of the EEPROM microchip. The chip will be delayered by different techniques after that. Optical images of the Cu chip will be captured during the delayering process. With sufficient project progress, SCM (scanning capacitance microscopy) through the use of AFM characterization will be executed to verify the reliability of the delayering technique as well as to ascertain the consistency of the programmable memory.

Equipment:
SEM (NTU)
Auto Decapsulator (NTU)
RIE (NTU)
AFM (NTU)

Remarks:
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