Job Description for Digital Design Engineer:

The candidate is expected to design and verify circuits, logic, systems, and algorithms to meet product requirements. Individual will determine the proper method and procedures to be used in the RTL/Digital system development and determine the best method for verifying the digital system before the complete design is committed to silicon. Candidate must have experience in implementing the proposed method and procedure to design and Verify ASIC digital circuits. Masters degree is a plus. SoC experience is also a plus.

Qualified in the following:

- Verilog design.
- Digital state machine architecture and logic design.
- Complex computational algorithm design and implementation in Verilog
- Verilog design verification.
- Multi-supply, multi-clock domain design
- Familiar with either Synopsys or Mentor Graphic design tools
- Creating/updating/maintaining fully-self-checking test benches using behavioral Verilog/VHDL.
- Performing synthesis and/or static timing analysis on complex designs.
- Communication Standards to Specification Translation, Verification methodologies (such as OVM, UVM and VMM) and DFT experience is a plus