Job description :
Analog Layout Design Engineer

Caeleste is a young and dynamic high-end, beyond state-of-the-art, image sensors supplier. We are focused on high performance imagers for scientific, medical and industrial applications. Caeleste is the originator or promoter of many novel concepts as indirect X-ray detection with photon counting, Color X-ray, and sub-0.5 noise electron read noise CMOS pixels. For our continuing growth we are looking for people who like to work on challenges beyond state of the art.

Job description

You will be working with a multi-discipline and international team of design engineers on innovative standard cell and pixel layout in the most advanced CIS process technologies. You will do the full custom layout and verification of complex standard cells. You will get responsibility over the Chip floor planning, pin placement and die area management, Pixel and periphery layout, Pad ring layout and ESD insertion, full-chip physical verification, tapeout, and mask data verification. You will setup or help to setup and manage the layout database.

Minimal requirements

- Being able to understand array layout specificity. Understanding the physical reason being Design Rule Checks, Layout versus Schematics verification and other physical and electrical design rules will be essential.
- Layout for low noise, low signal contamination
- The ability to read and understand complex designs
- Ability to take the challenge to handle all aspects of layout of chip.
- Ability to work as a team
- Creativity, analytical mind and problem solving skills
- BS or MS in Electrical Engineering, Mechanical Engineering, Physics or related field of study is required.

Additional skills that are of interest

- Demonstrable scripting/ design automation capabilities to improve productivity
- Ability to quickly interpret and repair complicated LVS and DRC problems using state of the art verification software
- Understanding of layout techniques for design-for-manufacture in advanced processes
- Associated Degree/certifications in CAD, engineering discipline, or IC design certification; or equivalent experience. 5 years previous experience preferred
- Prior work experience with Cadence, Tanner Ledit, pro-engineer, or other design environment and a good familiarity with physical verification tools (for example, Assura/Calibre/Ledit design rule check)
- Solid understanding of physical, electrical, and DFM rules for CMOS CIS processes, e.g. understanding lateral transistor structures and impact on latch-up
- be aware of traditional and modern, fine line CMOS design rules, ESD rules, impact of layout parasitics, manufacturing requirements and common layout verification techniques and tools.
- Experience in Analog/Mixed Signal full custom IC layout with a proven track record of full custom layouts in advanced CMOS technologies
- Good working knowledge of UNIX/Linux and scripting languages (e.g., TCL, c-shell, Perl) and EDA tools/methodology, such as synthesis, equivalency checking, static timing analysis
- Comprehension of isolation issues and ability to create effective shielding / isolation structures
- Experience with chip-level assembly and chip tapeout procedures

For all your questions, please contact Patrick Henckes, CEO of www.caeleste.be patrick.henckes@caeleste.be

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